A-1728
Part II

REPORT ONR-CR213-108-4F

AN INVESTIGATION OF PSEUDO ILS

W. E. Sears
E. R. Flynt
L. D. Holland
J. V. Vogt

Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

30 June 1976

Final Technical Report for Period 1 January 1975 – 31 May 1976

Prepared for
NAVAL ELECTRONICS SYSTEMS COMMAND
Washington, D. C. 20361

Office of Naval Research
Arlington, Virginia 22217

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: ONR-CR213-108-4F	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE *(and Subtitle)*: An Investigation of Pseudo ILS	5. TYPE OF REPORT & PERIOD COVERED: Final Technical, 1 JAN 75 - 31 MAY 76
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): W. E. Sears, J. V. Vogt, L. D. Holland, E. R. Flynt	8. CONTRACT OR GRANT NUMBER(s): N00014-75-C-1008
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Engineering Experiment Station, Georgia Institute of Technology, Atlanta, Georgia 30332	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62241N, RF 41-423-801-2,30, RMS 1423-801
11. CONTROLLING OFFICE NAME AND ADDRESS: Naval Electronic Systems Command, Washington, D. C. 20361	12. REPORT DATE: 30 June 1976
	13. NUMBER OF PAGES: 138
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)*: Office of Naval Research (211), 800 N. Quincy Street, Arlington, Virginia 22217	15. SECURITY CLASS. *(of this report)*: Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; Distribution Unlimited

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Radar — Pseudo ILS

Track-While-Scan — Landing Systems

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The overall objective of the MARCOR Radar Landing Systems program at Georgia Tech over the past four years has been to analyze the performance of aircraft landing systems of interest to the Navy. The work described herein was directed specifically toward investigating theoretically and experimentally the utility of the Pseudo ILS concept.

The investigation consisted of a design and implementation of the Pseudo ILS concept using an AN/TPN-8 precision approach radar supplied by the Marine

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

FOREWARD

The research on this program was conducted by the Systems Engineering Division of the Applied Engineering Laboratory, Engineering Experiment Station, at Georgia Tech.

This report is the Final Technical Report for Georgia Tech Project A-1728, sponsored by the Office of Naval Research (Code 211) under Contract N00014-75-C-1008. The work described was performed from 1 Jan 1975 through 31 May 1976. Earlier phases of this work had been performed under Georgia Tech Project A-1417 and Contract N00014-67-A-0159-0011 which commenced in April 1972. Technical reports concerning the project which have previously been published are: "Preliminary Study of Marine Aircraft Landing Systems", May 1973; "Analysis of AN/TPN-22 Antenna System", April 1974; and "MARCOR Radar Landing Systems Phase III", May 1975.

The program has been directed to be responsive in its research to areas of interest to the Naval Electronics Systems Command (NAVELEX), Marine Corps and Amphibious Electronics Division, in which Mr. Richard Wilz serves as Cognizant Engineer. The Cognizant Engineer at the Naval Electronic Systems Test and Evaluation Detachment (NESTED) is Mr. Preston Hopkins.

Mr. William E. Sears, III, served as Project Director for the work at Georgia Tech. The work was performed under the general supervision of Mr. Robert Zimmer, Chief of the Systems Engineering Division, and Dr. H. A. Ecker, Director, Applied Engineering Laboratory.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SECTION I

INTRODUCTION

1.1 Background

Military and civil aviation programs have a continuing requirement to improve the quality of terminal aircraft guidance systems. In the civil sector and some military operations air-derived systems (i.e., the instrument landing system (ILS) and the microwave landing system (MLS) have been used (or are planned for use) almost exclusively in the terminal guidance phase. The preference for air-derived guidance principally has been due to excessive pilot workload in responding to conventional ground-derived ground-controlled-approach (GCA) commands received aurally. In this report recent investigations by personnel of the Applied Engineering Laboratory at Georgia Tech of the "Pseudo ILS" concept are described. The concept uses ground-derived data from a precision tracking radar to amplitude modulate transmitters operating at the ILS frequencies with the appropriate frequency ratio (90 Hertz/150 Hertz) for proper course line and glide slope guidance displayed by the normal ILS needles. The concept relieves pilot workload due to aural communications, offers safer terminal phase guidance due to inherent GCA backup mode, and requires no modification to the airborne ILS equipment.

In the following paragraphs, the standard ILS system is reviewed and the Pseudo ILS concept is presented. Two elements of the Pseudo ILS system, the tracking unit and interface unit, are described in detail in later sections; preliminary test results also are summarized.

1.2 Existing ILS System

The ILS utilizes two space-stationary beams--a glide slope beam and a localizer beam. The glide slope provides vertical steering signals for landings in one direction (the front course) on the runway. The localizer provides lateral steering signals for front-course and back-course approaches to the runway. Marker beacons provide spot position checks at 4.5 miles range, at the 200-ft-altitude Category I decision height, and at the 100-ft-altitude Category II decision height along the front course.

The ILS glide slope antenna establishes a radiation pattern in space from which airborne ILS equipment derives a signal which is proportional to the vertical displacement of the aircraft from the glide path. This

signal drives the up-down cross-pointer needle in the aircraft. The normal glide path angle is established by the ground equipment between 2.0^{o} and 3.0^{o}, and the projected glide path intercepts the runway approximately 1000 feet beyond runway threshold. The localizer establishes a radiation pattern in space whose signal is proportional to lateral displacement from the vertical plane through the runway center line. This signal drives the left-right cross-pointer needle. Each glide slope channel is paired with a localizer channel so that both receivers can be tuned together. Acquisition normally occurs at a range of 15 nmi at 1000-ft. altitude or at a minimum enroute altitude (MEA). An audible identification signal and voice channel from the control tower are also provided via amplitude modulation of the ILS signals.

The glide slope carrier is modulated at 90 and 150 Hz in a spatial pattern that results in the percent modulation of the 90 Hz being larger than that of the 150 Hz at angles above the glide slope and vice-versa below the glide slope. The difference in percent modulations increases linearly with angular deviation from the glide slope. Predominance of the 150-Hz signal causes a "fly up" indication on the cross-pointer meter or flight director; predominance of the 90-Hz signal causes a "fly down" signal. Full scale deflection on the glide slope meter corresponds to $.7^{o}$ off glide slope.

The localizer course is aligned with the projected runway center line. The carrier is modulated at 90 and 150 Hz in a spatial pattern that results in the percent modulation of the 90 Hz being larger than that of the 150 Hz at angular displacements left of the course line and vice-versa for angles right of the course line. The differential percent modulations again increase linearly. The left-right cross-pointer meter shows "fly right" when 90 Hz predominates. A "fly left" indication is given when the 150 Hz signal predominates. Full-scale deflection on the localizer meter corresponds to 2.5^{o} off course.

Because the ILS radiation is continuous-wave (CW) reflections from terrain, buildings, aircraft (ground and airborne), and ground vehicles will reflect spurious energy to the landing aircraft. This can result in a bend, or scallop, in the course. When the localizer is installed, the antenna loop spacing and the current to each loop are adjusted to

place the nulls of the pattern along the directions to large obstructions. Screens are sometimes added behind the localizer to sharpen the front lobes and to reduce the side lobes selectively, at the expense of the back-course pattern.

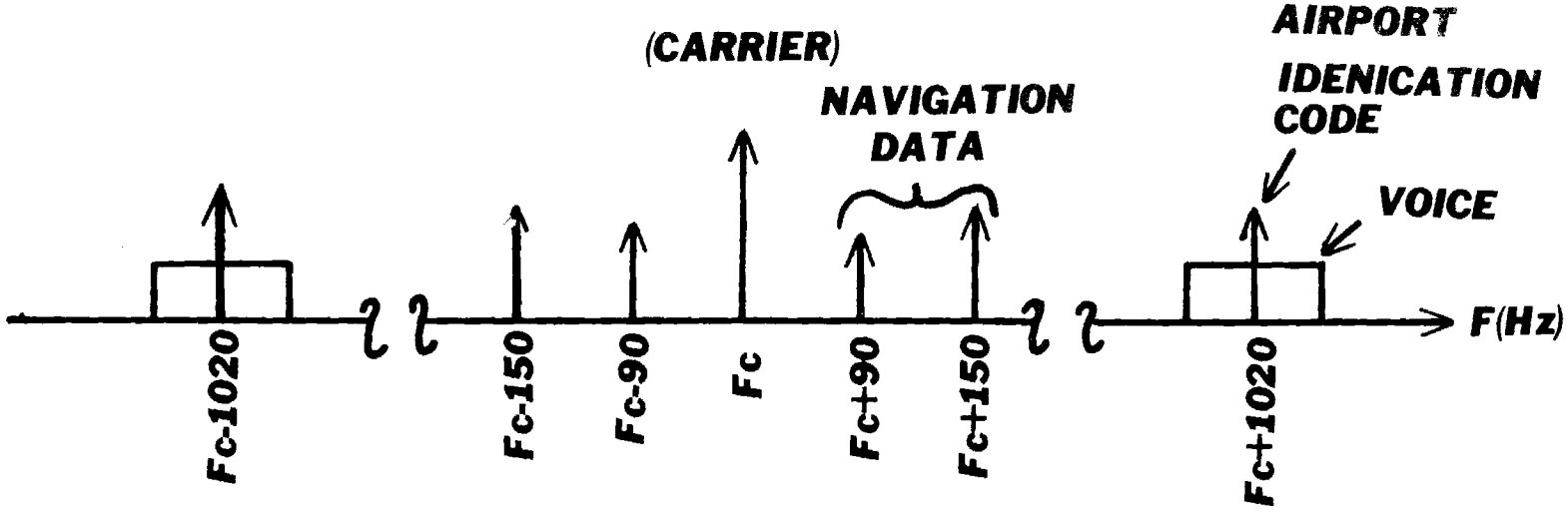
1.3 An Alternate Concept--Pseudo ILS

1.3.1 The Concept

Both the localizer and glide slope portions of ILS provide the aircraft with its deviation from the desired approach path by a difference in the depths of modulation of the 90-Hz and 150-Hz modulations on a carrier frequency. That is, the relative strengths of the 90-Hz and the 150-Hz modulations vary as a function of location around the approach path, with the variation being the result of a careful combination of normal transmitter amplitude modulation and the space modulation. The resultant ILS signal (say, that of the localizer) has a frequency spectrum as shown in Figure 1, with the location information contained in the difference in magnitude of the two tones 90 Hz and 1t0 Hz away from the carrier (normalized by the carrier magnitude).

The Pseudo ILS concept utilizes a ground-based tracking radar to determine the horizontal and vertical deviations from the desired path for a specific approaching aircraft, and then amplitude modulates that information onto carrier frequencies identical to those of an ILS and transmits them to the approaching aircraft. The aircraft ILS receiver interprets them as normal ILS signals; therefore any aircraft fitted for ILS operation is also capable of performing a Pseudo ILS assisted landing. Pseudo ILS does not suffer from the beam distortion problems of normal ILS and is therefore particularly attractive for airports with poor electromagnetic environments. The Pseudo ILS system can be extended to multiple aircraft capacity by using different ILS channels (carrier frequencies) for the different aircraft. Pseudo ILS systems can be set up rapidly and economically for small or emergency airfield use.

Still another method of conveying ground based radar approach data to the approaching aircraft is to replace the ILS receiver with a digital receiver capable of receiving and displaying range-to-touchdown data as well as the usual ILS display of left-right, up-down instructions. Such



INSTRUMENT LANDING SYSTEM (ILS)

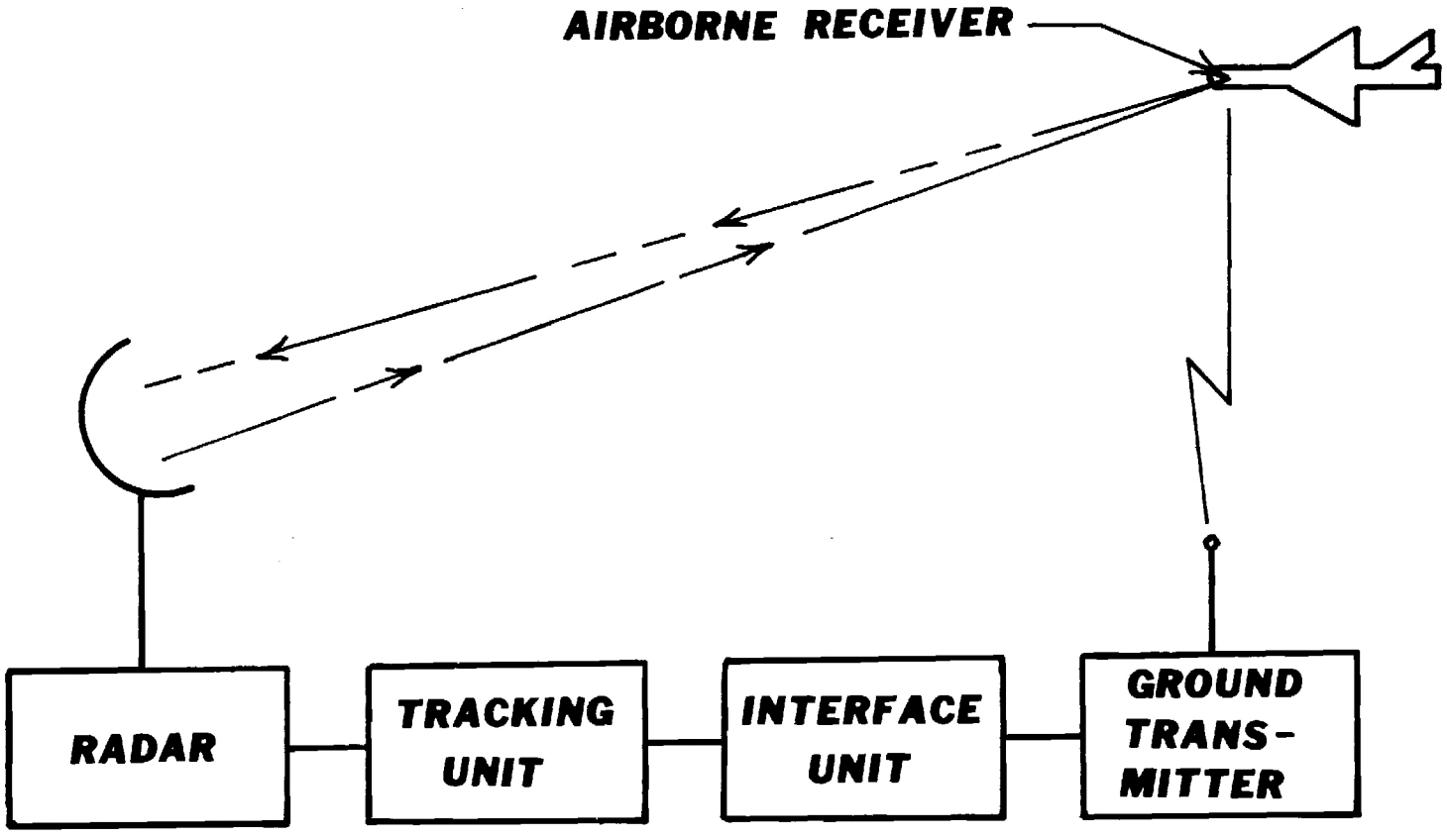
SIGNAL SPECTRUM AT RECEIVER INPUT

Figure 1. Instrument Landing System (ILS) Signal Spectrum at Receiver Input.

a system has been proposed and a prototype constructed by Republic, a division of Research Communications Industries. The tracker and the interface unit described in this report will operate with either the Pseudo ILS or the digital system.

1.3.2 Configuration

The basic elements of the Pseudo ILS are pictorially illustrated in Figure 2. The system consists of a radar, a tracking unit, an interface unit, a ground transmitter, and an airborne receiver. The Tracking Unit uses the radar output signals to track the approaching aircraft. A description of how the tracker performs its task is given in Section II. The investigation of Pseudo ILS has consisted of the design, construction, and test of the tracking unit and the interface unit. Detailed functional descriptions of these units are given in later sections of this report.



PICTORIAL ILLUSTRATION OF PSEUDO ILS CONFIGURATION

Figure 2. Pictorial Illustration of Pseudo ILS Configuration.

SECTION II

SIMULATION PERFORMANCE ANALYSIS

2.1 Introduction

A computer simulation of the Tracking Unit was developed to verify gain settings for proper transient (acquisition) response and steady-state error performance. In this section, tracking circuitry is presented in block diagram form, the tracking loop difference equations are given, a high-level simulation block diagram is described, and graphical results are presented for the particular gains selected for the representative scenario chosen.

2.2 Tracking Loop Definition

2.2.1 Range Loop

An s-plane block diagram of the range tracking loop is shown in Figure 3. The sampled-data system is characterized by a limiter, a relatively high speed sample-and-hold (SAH), a low-speed on-off switch, a second-order forward loop filter characteristic, and a unity feedback loop.

2.2.1.1 Components of the Loop

The circuitry is designed to provide for constant output between ε and ε_L in regions where the measured error is greater than half the radar's pulsewidth, $C\tau/2$. A piecewise-linear no-memory limiter, with limits at $C\tau/4$, is used to model this phenomenon.

The sampling time for the SAH, Ts_1, is set equal to the interpulse period of the radar, 833 microseconds. The on-off switch, S_2, allows the SAH output to drive the remainder of the loop only when the target is being illuminated by the radar. Other switching circuitry (not shown here) further confines range data to be utilized only when the target is illuminated by the elevation scanner for clutter reduction purposes. The switching time for S_2, T_{s2}, then is determined as the time between successive target illuminations by the elevation beam.

The beam is scanned sinusoidally with a period of 2 seconds, and the target is successively illuminated with the beam scanning in opposite directions. Alternate switching times for S_2 then are determined by the elevation angle of the target, i.e., equal off target scan times of 1 second occur only when the target elevation coincides with the middle of the elevation scan sector.

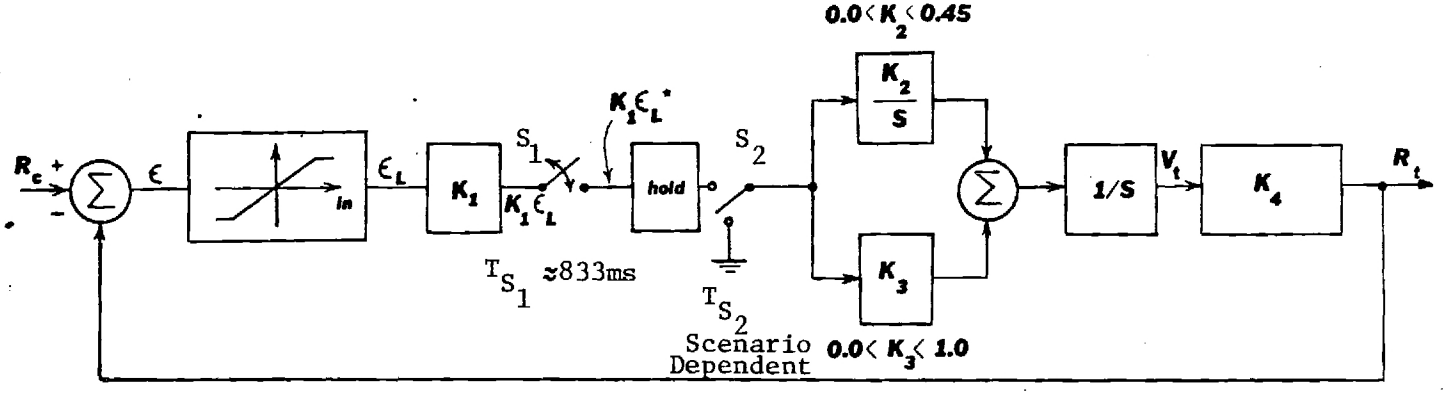


Figure 3. Block Diagram of Range Tracking Loop.

Between scans, S_2 grounds the SAH output so that the input to the second integrator is a constant and V_t in Figure 3 is a linear ramp.

2.2.1.2 Operation of the Loop

The adjustable gains, K_2 and K_3, are chosen to permit loop operation in the following manner. During the dwell time of approximately 25 milliseconds, the high forward loop gain combination of $K_1K_3K_4$ dominate gate movement and exhibit a closed loop response time of a few milliseconds with midrange setting of K_3. Gain K_2 has negligible effect during the target dwell time due its relative brevity compared to the interscan period (Ts_2:Ts_1≃38:1). During the interscan period, the loop is opened via S_2 switching to ground. The ramp output described in 2.1.2 is driven by the small constant voltage derived by the K_2 integrator during the dwell time. The output of K_3 is zero during the interscan period.

The transient response of the loop within a single dwell time then is determined essentially by K_3. Between scans, the gate is driven open loop at a constant rate determined by K_2. The range tracking loop difference equations are given in Figure 4.

2.2.2 Angle Loops

An s-plane diagram of the identical azimuth and elevation angle tracking loops is shown in Figure 5. The s-plane diagram is identical to that of the range loop with the exception that only one sampler is used.

2.2.2.1 Components of the Loop

The piecewise-linear no-memory limiter is used with limits at $\pm\theta_B/2$. Its operation is identical to that of the range loop.

The sampling time, Ts, is flight path dependent since the system is a bidirectional, track-while-scan tracking system. When tracking near the center of the scan sector, Ts is nearly the same scan-to-scan. When tracking near the sector edge, alternate sampling times can approach a 3:1 ratio. The effect is to increase scan-to-scan tracking error since appropriate tracking loop gain settings are sampling rate dependent. Tracking loop performance is better, however, than that achieved by only sampling at every other opportunity, i.e., unidirectional, constant-sample-rate sampling at approximately one-half the average bidirectional sampling rate.

RANGE-TRACK DIFFERENCE EQUATIONS

(LIMIT TO $\pm$ .008 NMI)

$$(\epsilon_L^*)_N = \left[(R_C)_N - (R_T)_{N-1}\right]_L$$

$$(V_2)_N = (V_2)_{N-1} + (K_1 K_2 T_S)(\epsilon_L^*)_N$$

$$(R_T)_N = (R_T)_{N-1} + (K_4 T_S)(V_2)_{N-1}$$

$$+ K_1 (K_4 T_S)\left[K_3 + K_2 T_S/2\right](\epsilon_L^*)_N$$

Figure 4. Range Track Difference Equations.

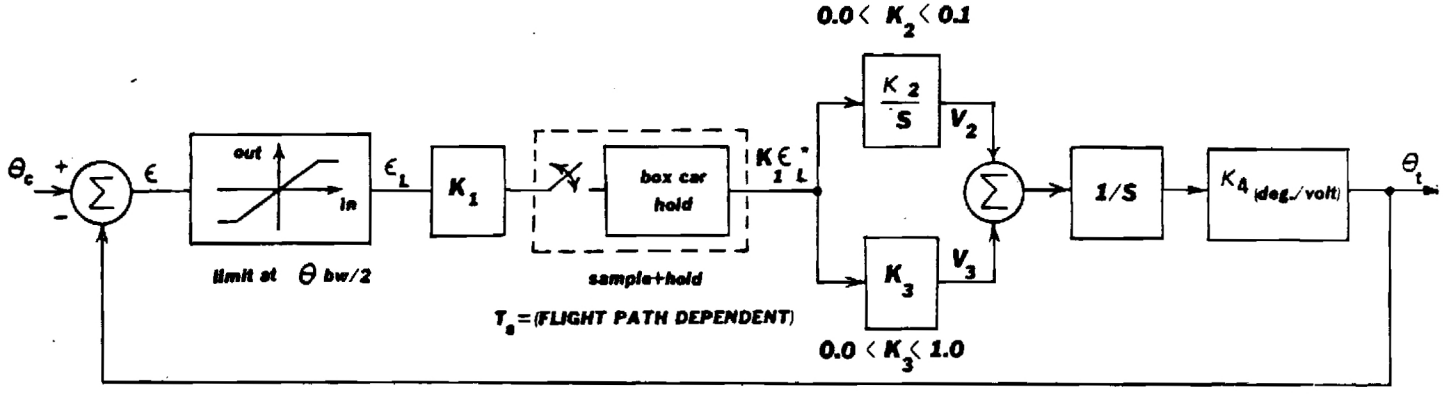


Figure 5. Block Diagram of Angle Tracking Loop

2.2.2.2 Operation of the Loop

In contrast to the range loop, both K_2 and K_3 continuously affect loop response. The sampled-and-held error voltage exists at all times, changing at a scan-to-scan rate. Midrange gains on K_2 and K_3 are chosen, however, to enable the short-term response to be dominated by K_3. and the long-term (several scan memory) response to be determined by K_2. The angle tracking loop difference equations are given in Figure 6.

2.3 Simulation Description

2.3.1 The Computer Program

A high-level block diagram of the tracking system simulation and program is shown in Figure 7. An executive routine controls all input/output timing for the simulation and allows the analyst to change simulated parameters in a conversational manner. True target range, azimuth, and elevation are updated at appropriate rates depending on the desired outputs. For example, range gate transient acquisition response requires updates at the pulse repetition rate, whereas angle gate transient acquisition response requires updates only at the much slower scan rate.

Imperfect measurement of the true target coordinates is simulated by addition of Gaussianly distributed random variables with rms values equal to some fraction of the radar's range and angular resolution. Tracking errors are derived by subtracting tracker output coordinate estimates from the true coordinates.

2.3.2 Input Data

2.3.2.1 Flight Profile

A standard 3° glide slope was assumed for the simulation runs. The aircraft was assumed on course, and was flown to touchdown. The touchdown point offset from the radar was adjustable. For the results shown in this section, the down range distance was 800 feet with an offset perpendicular to the runway of 400 feet.

2.3.2.2 Tracking Loop Gains

The tracking loop gains used to produce the results shown in this section are given in Table 1. Extensive sensitivity analysis to achieve optimum response was not accomplished due to time constraints. The parameter values shown produced stable responses.

$$(\epsilon^{*}_{L})_N = \left[(\theta_c)_N - (\theta_t)_{N-1}\right]_{\text{LIMITED}}$$

$$(V_2)_N = (V_2)_{N-1} + (K_1 K_2 T_s)(\epsilon^{*}_{L})_N$$

$$(\theta_t)_N = \left\{(\theta_t)_{N-1} + K_4 T_s (V_2)_{N-1} + K_1 K_4 T_s \left[K_3 + K_2 T_s/2\right](\epsilon^{*}_{L})\right\}$$

Figure 6. Angle Track Difference Equations.

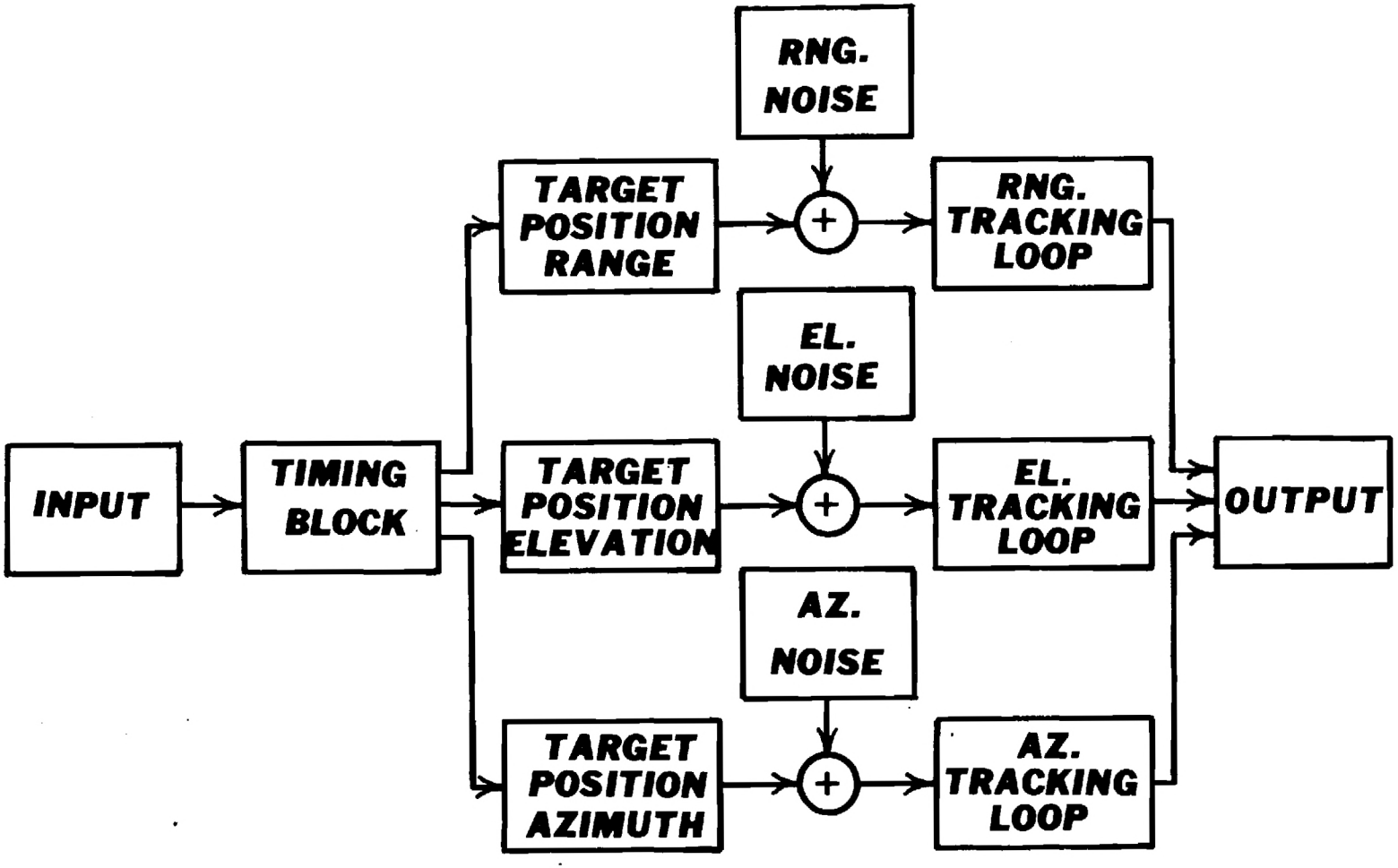


Figure 7. Simulation Block Diagram.

TABLE I

TRACKING LOOP GAINS FOR SIMULATION

	RANGE	AZIMUTH	ELEVATION
K1	2417	2.8	8.5
K2	.441	.020	.008
K3	.888	.150	.050
K4	.4	1.0	1.0

2.4 Simulation Results

2.4.1 Transient Responses

Transient responses to a step input to the range, azimuth, and elevation tracking loops are shown in Figures 8, 9, and 10, respectively. The two curves in each figure represent responses to inputs with magnitudes above and below the value required for error limiting. The responses show stable loop response times on the order of five milliseconds (≈six interpulse periods) for range and eight seconds (≈sixteen interscan periods) for both azimuth and elevation.

2.4.2 Precision Approach Response

Loop responses during a simulated precision approach are shown in Figures 11 through 16.

2.4.2.1 Range Loop

Range gate error versus time with noise-free radar measurement and noisy radar range measurement are shown in Figures 11 and 12, respectively. The breaks in the abscissa indicate off-target scan intervals. It can be seen that, even under noisy measurement conditions, a firm range gate lock-on with very small initial error is achieved within three scans across the target. The simulated target velocity was 120 knots. The results shown are for the case of no *a priori* velocity prediction. If the approach velocity is approximately known, as is usually the case, the firm track is established normally within one scan. Only the initial portion of the approach is shown since an excellent track was maintained for the remainder of the approach. The curves shown are very typical of the responses recorded over a broad range of variation in the simulated profile.

2.4.2.2 Angle Loops

Angle gate error versus time with noise-free and noisy radar angle measurement are shown for azimuth in Figures 13 and 14, respectively, and for elevation in Figures 15 and 16, respectively. The responses are very similar for azimuth and elevation in the respective cases of noise-free and noisy radar angle measurement. The major difference in the responses is the effect of non-uniform sampling in elevation as opposed to uniform sampling in azimuth. As previously discussed, this phenomenon is flight path dependent, and the factors of 3° glide slope and the offset of the radar from the touchdown point result in the phenomenon being more pronounced

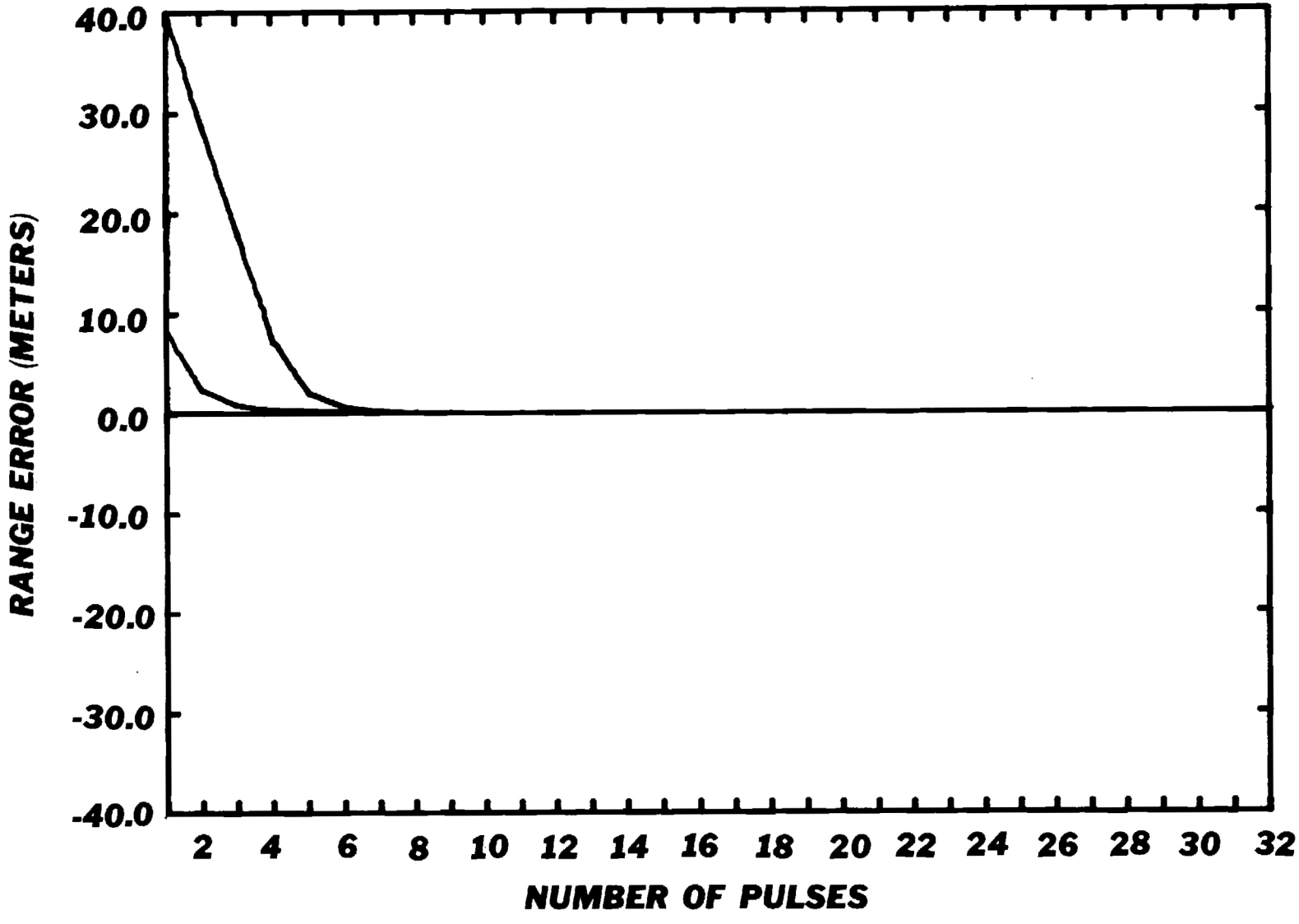


Figure 8. Range Gate Transient Response

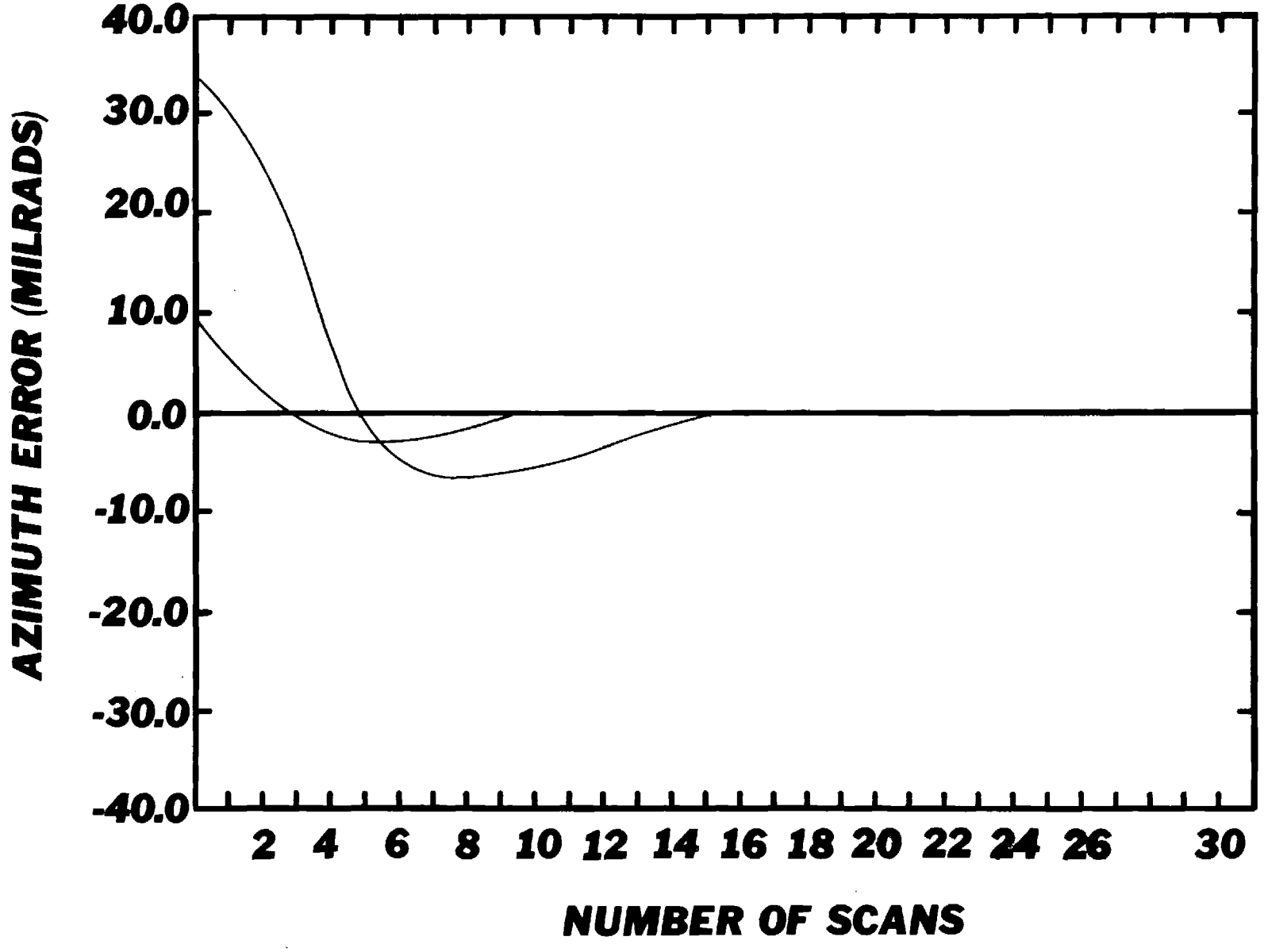


Figure 9. Azimuth Gate Transient Response.

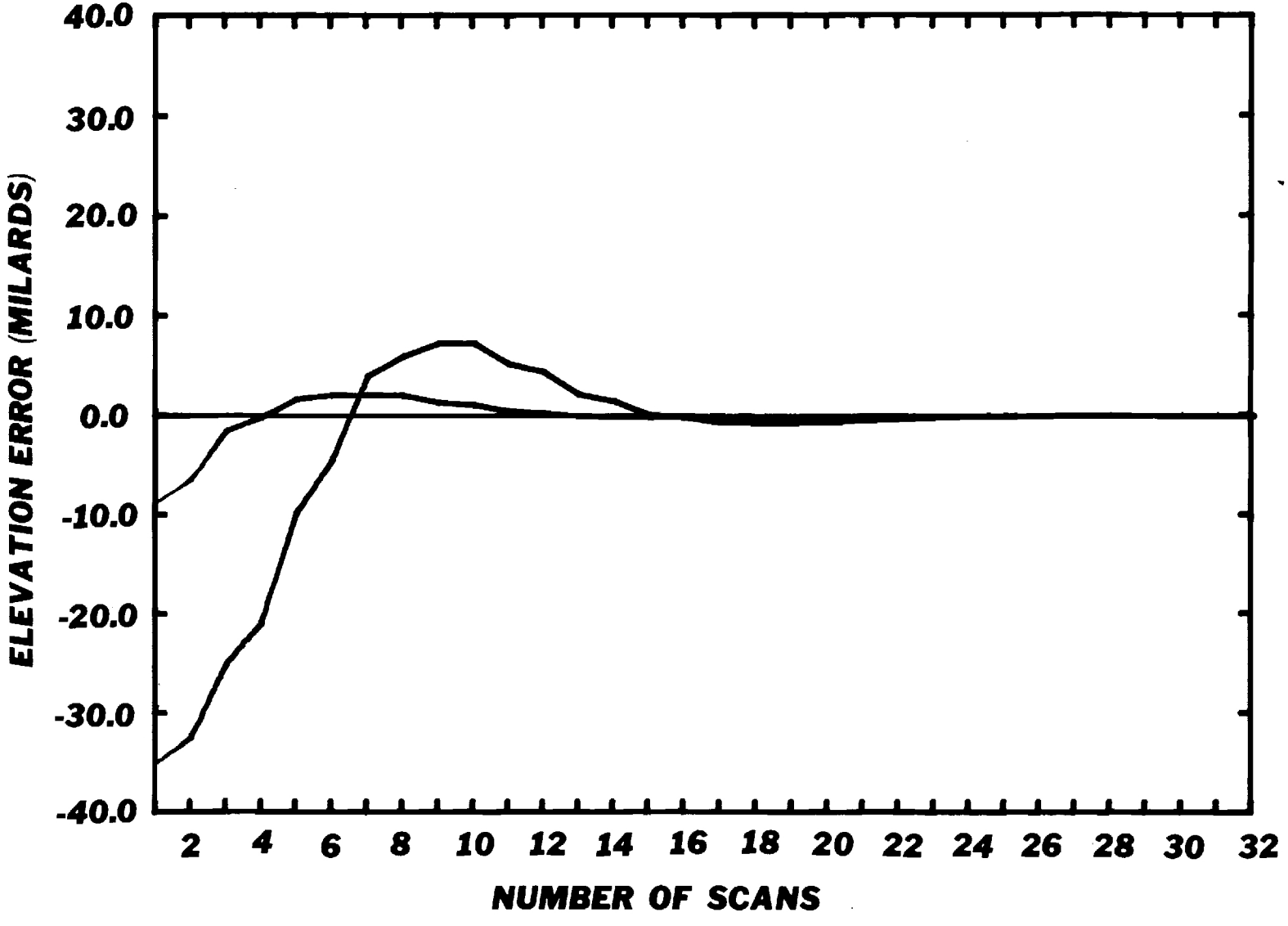


Figure 10. Elevation Gate Transient Response.

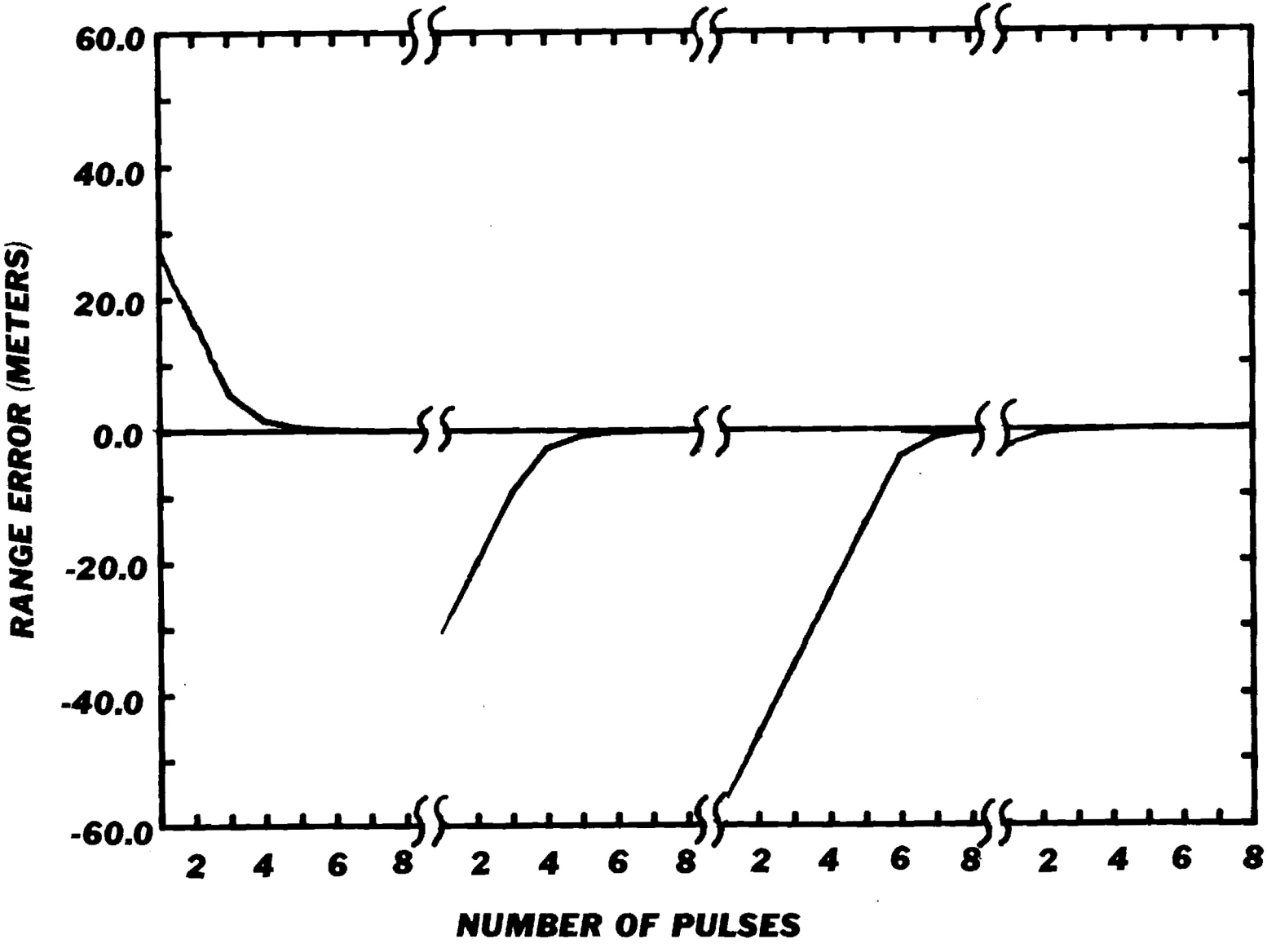


Figure 11. Range Error During Acquisition, Noise-free Radar Measurement.

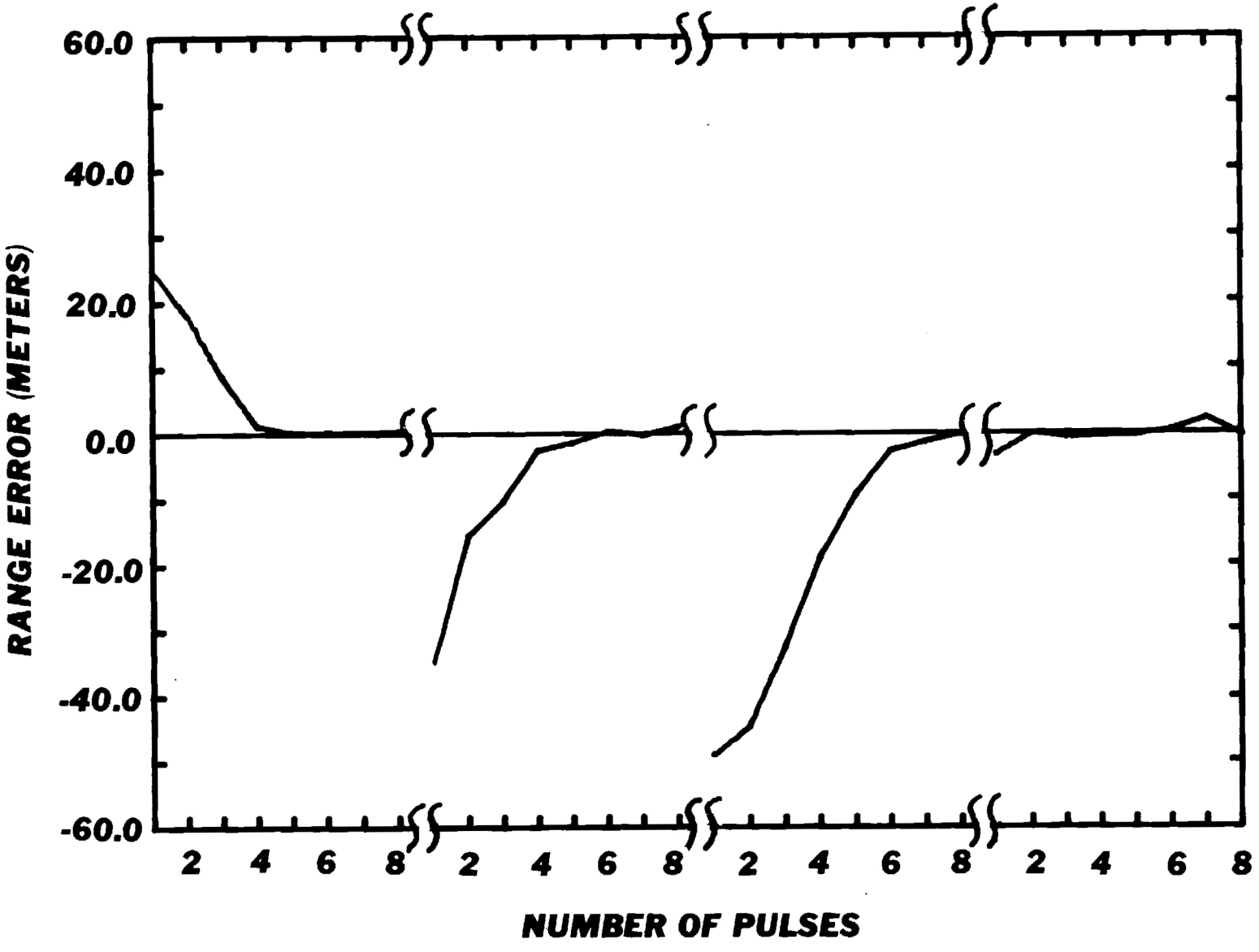


Figure 12. Range Error During Approach, Noise Radar Measurement.

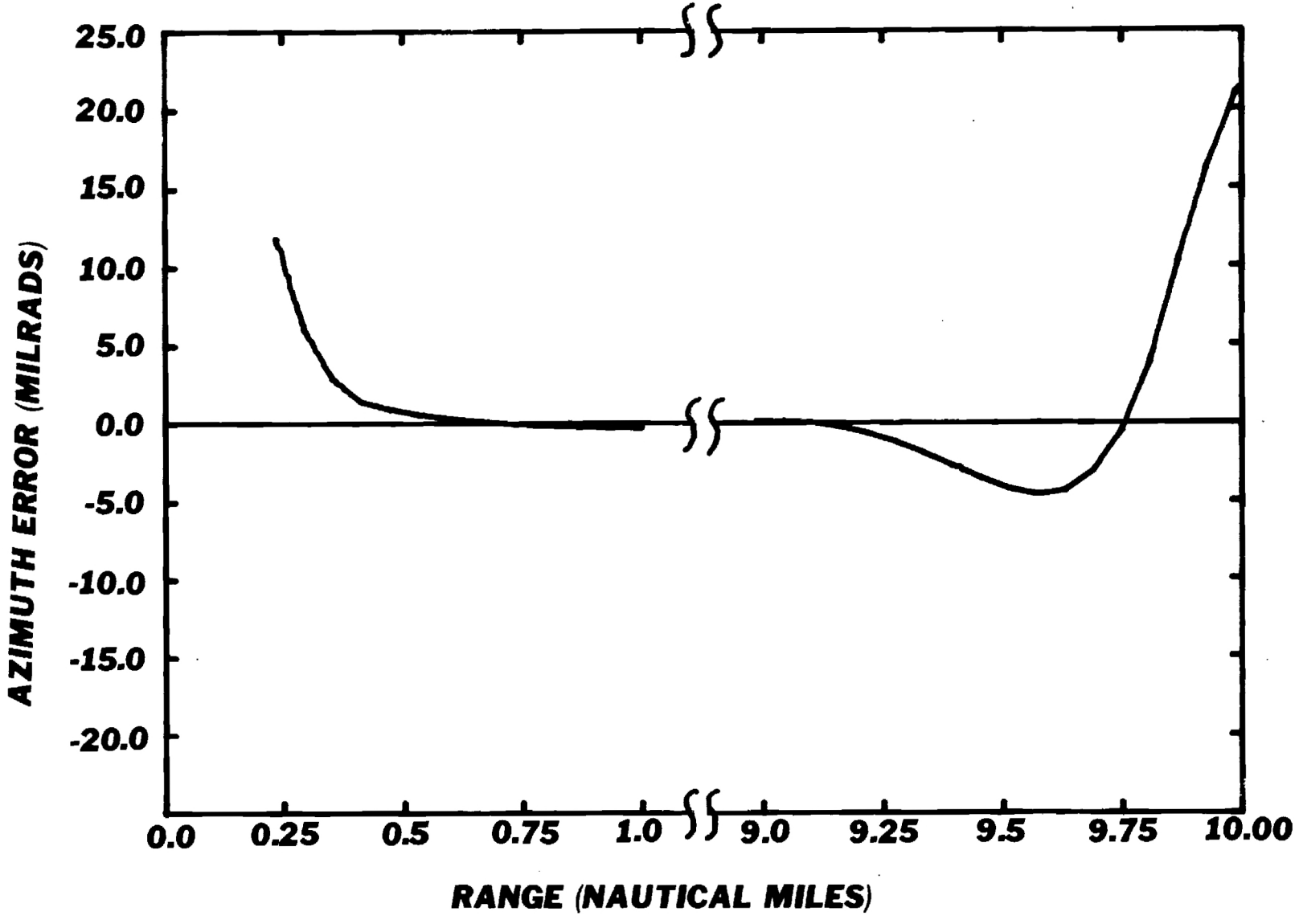


Figure 13. Aximuth Error During Approach, Noise-free Radar Measurement.

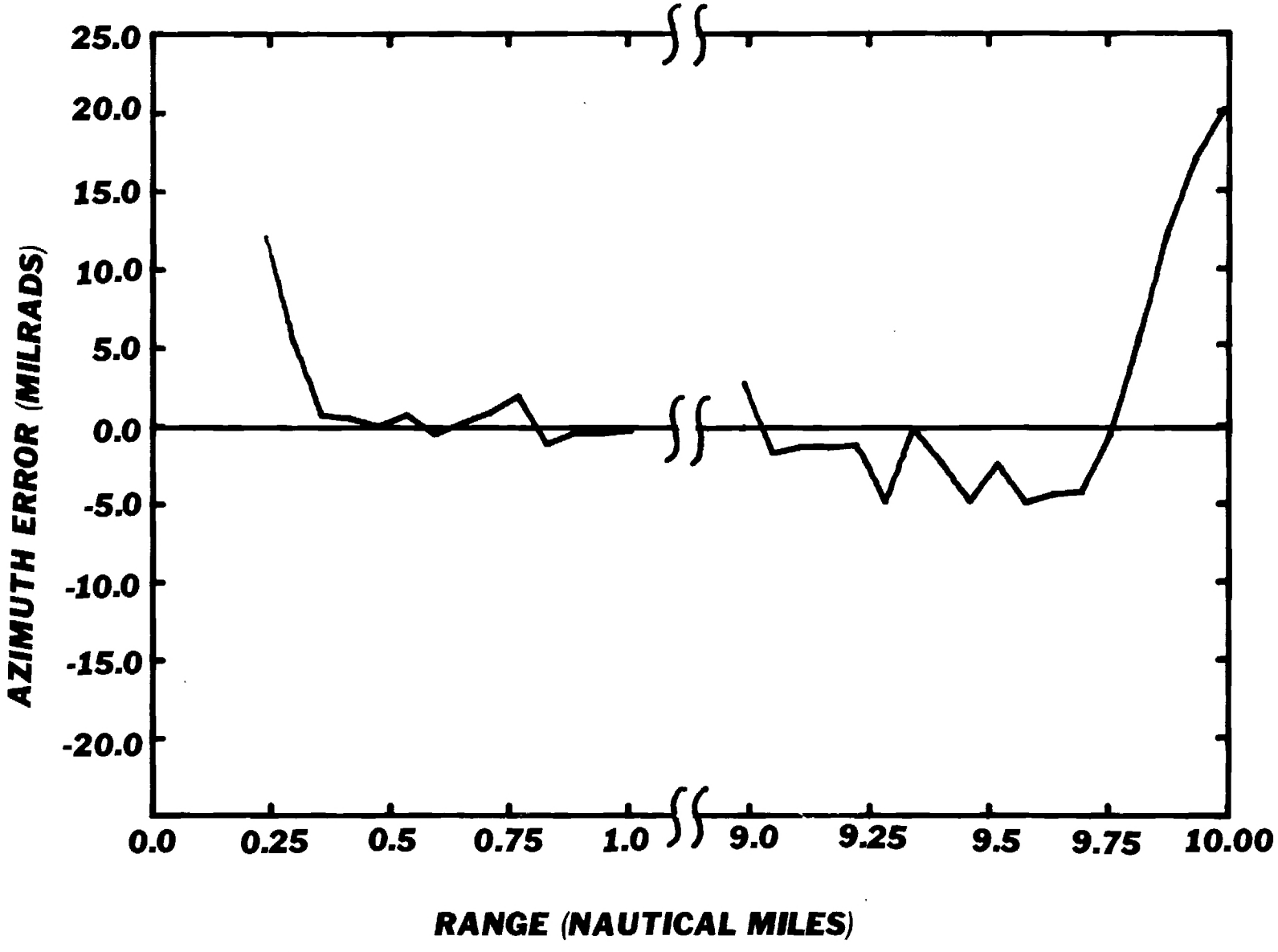


Figure 14. Azimuth Error During Approach, Noisy Radar Measurement.

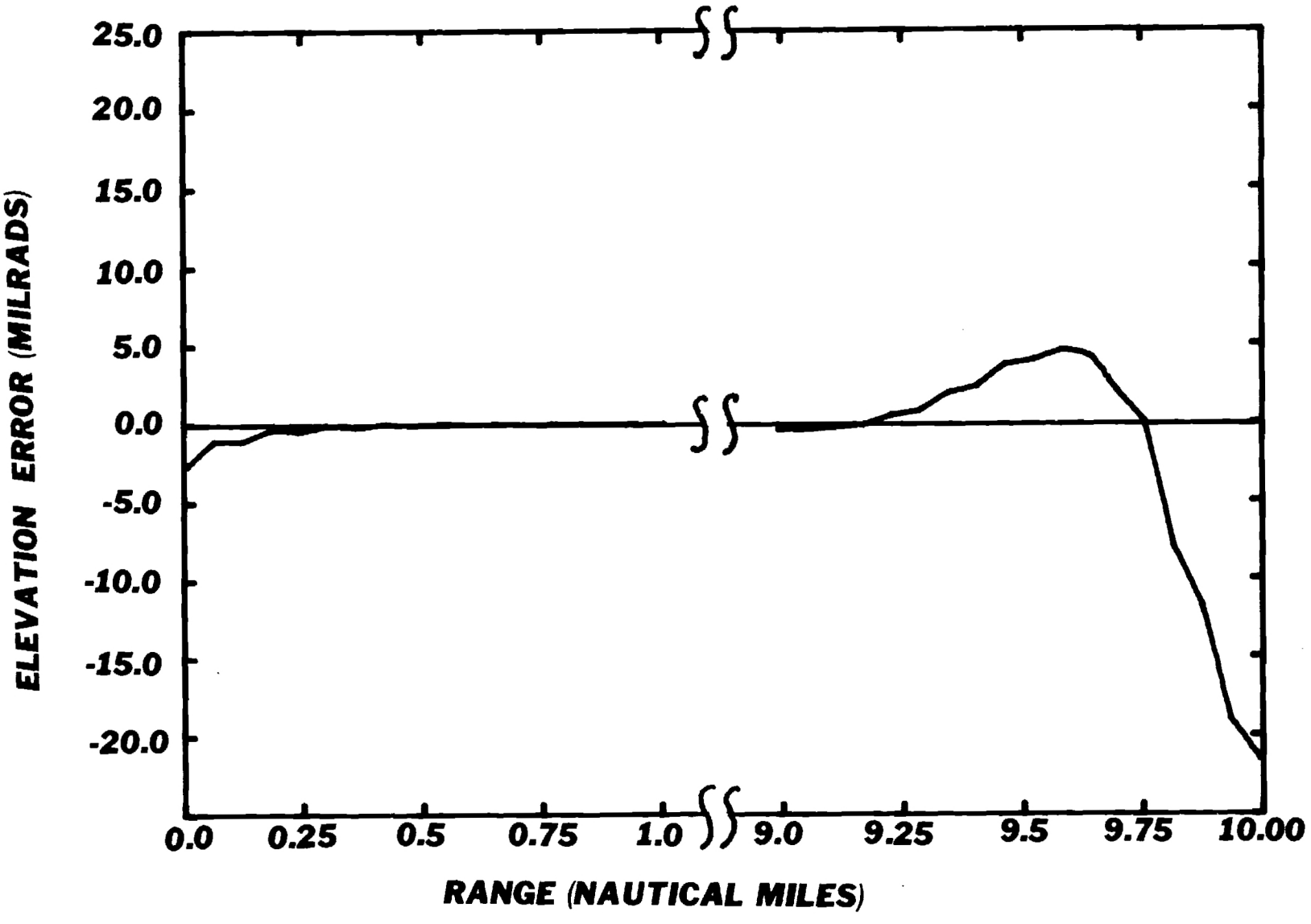


Figure 15. Elevation Error During Approach, Noise-free Radar Measurement

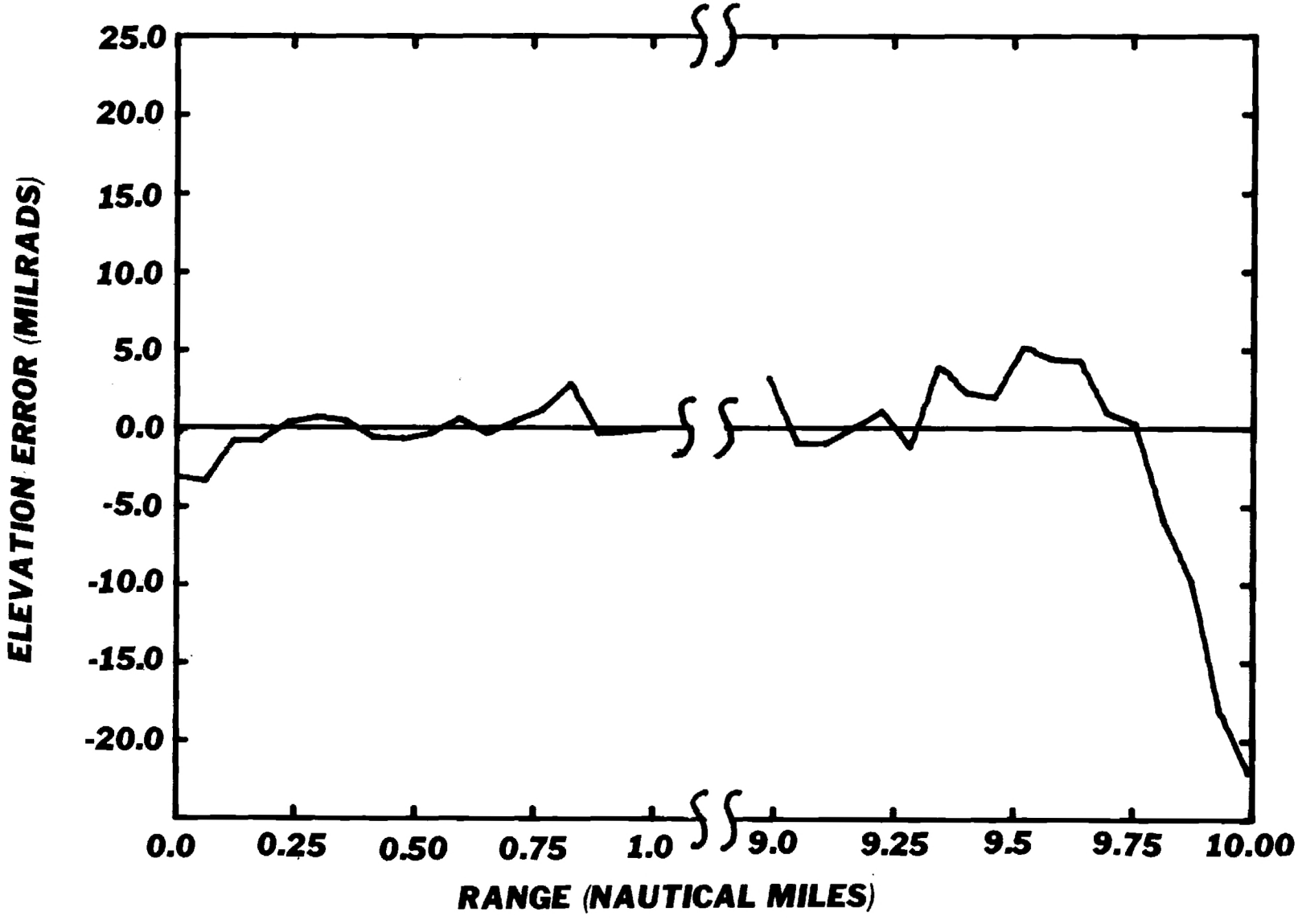


Figure 16. Elevation Error During Approach, Noisy Radar Measurement.

in elevation than in azimuth. The break in the abscissa represents the mid portion of the flight in which the relatively slow angular variation with time resulted in a very good mid approach track. Toward the end of the approach, the offset of the radar from the touchdown point again produced an effect. At the terminal portion of the flight (inside 0.5 nmi. from touchdown) the azimuth angle began to increase rapidly with time, producing the large error in azimuth at touchdown. The elevation change with time was much less and produced less error. These results reflect gate errors with no provision for a priori radar offset error computation. Such computation would reduce these errors to a negligible amount. The angle error curves shown also are very typical of the results obtained over a broad range of variations in the simulated profile.

SECTION III

TRACKING UNIT TECHNICAL DESCRIPTION

3.1 Introduction

The purpose of the Tracking Unit is to use radar output signals to perform the task of tracking the approaching aircraft. This section includes a functional description of the Tracking Unit by Sub Units and a detailed description of the circuits on a board-by-board basis.

3.2 Functional Description

A block diagram of the Tracking Unit is shown in Figure 17. A description of how the tracker performs its tracking task is best given in terms of its eight sub units which perform individual functions. Seven of the sub units consist of one or more cards; the eighth sub unit consist of the front panel controls. The eight sub units, by function, are the following:

1. Input Signal Conditioning,
2. Automatic Target Acquisition,
3. Range Tracking,
4. Azimuth Tracking,
5. Elevation Tracking,
6. Output Signal Conditioning,
7. Simulated Target Generation, and
8. Front Panel Controls.

In the following paragraphs, these sub units are described more fully.

3.2.1 Sub Unit No. 1 - Input Signal Conditioner

The Input Signal Conditioner accepts as input three, low-bandwidth, angle timing signals normally sent from the master indicator to the slave indicator and two pulse type signals received directly from the receiver-

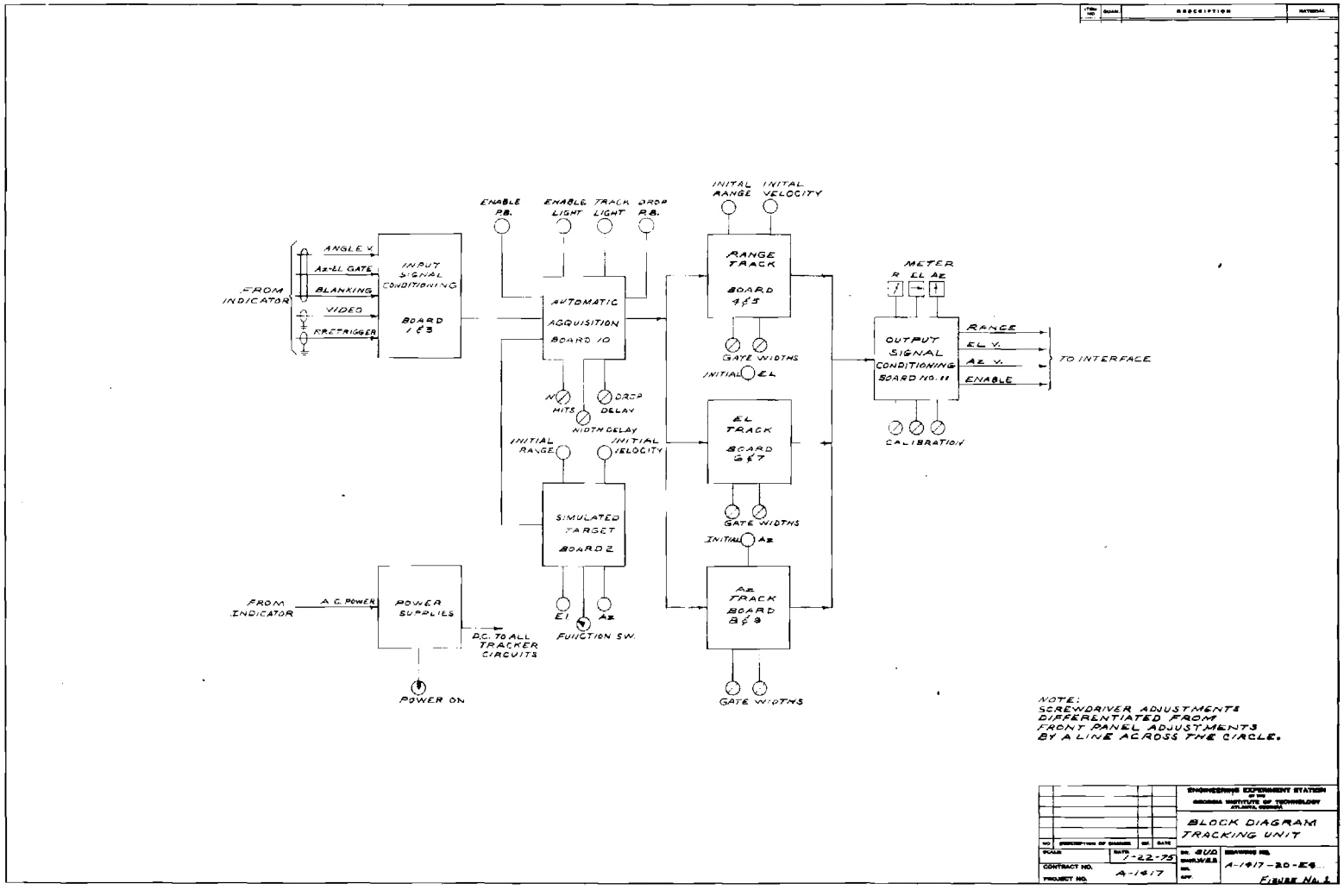


Figure 17. Block Diagram of Tracking Unit.

transmitter. These inputs are the following:

a. Angle Volts - a timing signal which gives a unique indication versus time of the position of the two scanning antennas when these antennas are within their normal scan sector,

b. Azimuth - Elevation Gate - a timing signal which indicates which of the two time-multiplexed scanning antennas is scanning through its normal sector at a given point in time,

c. Unblanking Gate - a timing signal which blanks the return video during the interval in which one scanning antenna has completed a traverse of its normal scan sector and the other antenna has not begun to scan its next normal sector, (scan transition time),

d. Video - the detected return from the radar targets, and

e. Pretrigger - a timing pulse which sets a reference for timing within each interpulse period.

The processing performed on each of these inputs is described below.

The Angle Volts signal is impedance buffered and transmitted with unity gain to the Simulated Target Generator, the Azimuth Tracker, and the Elevation Tracker.

The Azimuth-Elevation Gate is converted to logic levels and inverted. The non-inverted logic signal is transmitted to the Simulated Target Generator and the Azimuth Tracker. The inverted signal is transmitted to the Elevation Tracker.

The Unblanking Gate signal is converted to logic levels, impedance buffered, and transmitted to the Simulated Target Generator, the Azimuth Tracker, and the Elevation Tracker.

The Video signal is processed differently, depending on whether the tracker is on or off. If the tracker power is off, the video is passed through, unchanged, to the master indicator. If tracker power is on, the video is summed with the simulated target video, the azimuth tracking gate, and the elevation tracking gate. The composite signal is then compared with a threshold for noise immunity and transmitted to the master indicator.

The Pretrigger signal is converted to logic levels, passed through a trigger hold-off circuit, and transmitted to the Simulated Target Generator and the Range Tracker. The function of the trigger hold-off circuit is to eliminate the possibility of false pretriggers due to multiple reflections

in the pretrigger cable resulting from impedance mismatches.

A final function of the Input Signal Conditioner is to generate the +12 and -6 volt supplies from the +15 and -15 volt power supplies.

3.2.2 Sub Unit No. 2 - Automatic Target Acquirer

The Automatic Target Acquirer accepts the following six inputs:

1. logic level video which is range and elevation gated and stretched,
2. the elevation gate,
3. logic level video which is range and azimuth gated and stretched,
4. the azimuth gate,
5. positive, logic level pulse resulting from momentary push of ENABLE button on front panel, and
6. positive, logic level pulse resulting from momentary push of DROP button on front panel.

The Automatic Target Acquirer uses these inputs to derive two output signals as described in the following paragraphs.

One output is the Acquisition Gate signal which determines whether or not the automatic acquisition and tracking circuits are enabled to perform their function. A momentary push of the DROP button on the front panel forces the Acquisition Gate signal to the HOLD (high) level. The circuitry latches the signal in the HOLD state until the ENABLE button on the front panel is pushed. At this time the signal transitions and latches in the TRACK (low) state.

When in the TRACK state, the acquisition circuitry is enabled to perform its function as follows. Gating and integrating circuitry are used to determine when at least N threshold-exceeding video pulses have occurred within the wide range and angle gates on the last scan of each antenna in succession in either order. The Number N is determined by a screwdriver adjustment labeled HITS TO ACQUIRE.

Existence of this state of conditions is indicated by a logic signal, ACQ (high when in this state), which is integrated and compared to an adjustable threshold. When the integrated output exceeds the threshold, a signal is generated which effects a transition of all tracking gate widths to the smaller

value to be used during track. The delay in going from wide acquisition gate widths to narrow tracking gate widths is determined by a screwdriver adjustment labeled NARROW GATE DELAY. This WIDE/NARROW logic signal is the second output from the Automatic Target Acquirer.

The circuitry also allows for automatic track drop as follows. The logic signal ACQ is averaged over several scans and compared to an adjustable threshold (screwdriver adjustment) labeled DROP DELAY. If ACQ goes low (loss of target) for M scans (adjustable with DROP DELAY), the Acquisition Gate output will transition to and latch in the high state. Again, the acquisition and track functions then are disabled until the ENABLE button on the front panel is pushed.

3.2.3 Sub Unit No. 3 - Range Tracker

The Range Tracker accepts as inputs an Acquisition Gate and a Gate Width Select Signal Automatic Target Acquirer, a reference timing pulse from the Input Signal Conditioner, and the threshold video from the Input Signal Conditioner. The processing is as follows.

The Acquisition Gate enables or disables the range tracking function. The disabling process clamps the tracking gate velocity to zero and forces the tracking gate position to a point in range chosen with front panel controls (normally the desired initial acquisition range).

The reference timing pulse is used to begin a ramp voltage which becomes the range reference signal to identify the range of the incoming thresholded video. The range reference signal is compared to the output of the Range Tracker. As the ramp passes the current gate position, a pulse is generated which begins a second ramp. The second ramp is compared to five reference voltages corresponding to (1) the beginning of the Wide Range Gate, (2) the beginning of the Narrow Range Gate, (3) the center of the Range Gate, (4) the end of the Narrow Range Gate, and (5) the end of the Wide Range Gate.

Pulses are generated for each of these five points in range. The Gate Width Select signal is then used to allow the appropriate pulses to set and reset flipflops to generate either Wide or Narrow versions of the Early Gate, Late Gate, and Total (Early and Late) Range Gate.

The tracking loop is a conventional split-gate range tracker with a second

order characteristics equation. The loop has velocity memory and is tailored to constant-velocity flight profiles. Provision is made to aid initial automatic acquisition by inserting any a priori information about the aircraft's velocity.

The Range Tracker outputs stretched (sampled and held for one interpulse period), range-gated video to the Azimuth and Elevation Angle Trackers.

3.2.4. Sub Unit No. 4 - Azimuth Angle Tracker

The Azimuth Angle Tracker accepts as inputs from the Input Signal Conditioner the Az-El Select signal, the unblanking signal, and the Angle Volts signal; from the Automatic Target Acquirer, it accepts the Acquisition Gate and Gate Width select signal; from the range tracker, it accepts the stretched, range-gated video.

The Az-El Select signal allows the stretched, range-gated video to be processed only during the azimuth scans; the unblanking signal insures that no video is processed while the system switches between scanners.

The Acquisition Gate and Gate Width Select signal perform identical functions to those in the range tracker, namely, enabling or disabling tracking operation and selection of Wide or Narrow gate widths, respectively.

The Angle Volts signal is the reference signal which identifies the azimuth angle of the incoming stretched and range-gated video. The angle reference signal is compared to the output of the Azimuth Angle Tracker. The difference in the two signals is compared to reference voltages located symmetrically about zero, which, with appropriate gating, generate the equivalent plus (+) and minus (-) angle gates used in the split-gate angle tracker. The terminology "plus" and "minus" is used since the gates are generated on one scan from left-to-right and on the following scan from right-to-left. Therefore, a time-based "early-late" technique could not be used--hence the fixed reference voltage technique.

A measure of the video occurring in each gate is obtained and the difference is the error voltage in the azimuth angle tracking loop. As in the case of range, the tracking loop is a split-gate tracking scheme with a second order characteristic equation.

3.2.5. Sub Unit No. 5 - Elevation Angle Tracker

The Elevation Angle Tracker is identical in design to the Azimuth Angle Tracker. Inputs are common between them and the gating and loop descriptions

are identical. The single difference of some consequence is that the Elevation Angle Gate is used to angle gate the video seen by the Range Tracker. This procedure is intended to reduce the amount of ground clutter with which the tracker must contend.

3.2.6 Sub Unit No. 6 - Output Signal Conditioner

The Output Signal Conditioner accepts as inputs the Range Tracker output, the Azimuth Tracker output, the Elevation Tracker output, and the Gate Width Select Signal.

The Range Tracker output is differenced with the Range Zero reference voltage, a screwdriver adjustment, and the difference is amplified with another screwdriver adjustable gain. This analog signal is outputted to the Interface.

The Azimuth and Elevation Tracker outputs are processed identically. Each is differenced with a reference voltage which is set by potentiometers on the front panel. The difference is then amplified with a screwdriver adjustable gain. These analog signals are then outputted to the interface and meters on the front panel.

The Gate Width Select signal is inverted and outputted to the interface as a Disable/Enable signal. This method is used to insure that guidance data is transmitted only when the tracking unit is in the TRACK (Narrow Gate) mode.

3.2.7 Sub Unit No. 7 - Simulated Target Generator

A Simulated Target Generator was incorporated to aid in tracker alignment and trouble shooting. It is also useful for demonstration of the tracker's operation.

The Simulated Target Generator accepts its inputs from the Input Signal Conditioner and Front Panel Controls. It receives from the Input Signal Conditioner a reference timing pulse, the Az-El Select logic signal and its inverse, the Unblanking signal, and the Angle Volts signal. It receives from the Front Panel Controls the desired Initial Range, Azimuth, and Elevation of the simulated target. Also received from the Front Panel controls is a RUN/RESET signal which causes the Simulated Target to either close in range at a speed selected on the front panel or reset to the Initial Range also set by a Front Panel control.

The Az-El Select and Unblank signals are used as in the angle tracking sub units to pass the simulated video during the appropriate portions of the angular

sweeps.

The Angle Volts signal is differenced with the desired azimuth (courseline) and elevation (glideslope) for the simulated target. The desired angles are set in with potentiometers on the front panel. The differenced outputs are compared with reference voltages to generate gating signals which determine the azimuth and elevation extents of the simulated target. These width (azimuth) and height (elevation) dimensions are screwdriver adjustments. These signals then gate appropriately the synthetically generated video to simulate target returns at the desired azimuth and elevation angles.

The synthetic video is generated by using the reference timing pulse to begin a ramp voltage which is compared to the Simulated Target range voltage, the comparator output being differentiated at the point of crossover. The resulting pulse triggers a controllable-width one-shot circuit which generates the synthetic video. The video width is a screwdriver adjustment.

The output from the Simulated Target Generator is summed directly with the thresholded radar video return in the Input Signal Conditioner and is processed by the tracker as normal video.

3.2.8 Sub Unit No. 8 - Front Panel Controls - Figure 18

The Front Panel Controls of the Tracking Unit are itemized below with a brief description of their individual functions.

3.2.8.1 Acquisition Controls

3.2.8.1.1 Acquisition Gates - determine initial settings for the following acquisition window parameters:

1. Elevation,
2. Azimuth,
3. Range, and
4. Velocity;

3.2.8.1.2 Power Switch - on/off switch for tracking unit only;

3.2.8.1.3 Enable Button - enables acquisition and track sequence to begin on any video within the Acquisition Gates;

3.2.8.1.4 Drop Button - interrupts acquisition or track sequence and latches in "dropped" state until the Enable Button is depressed.

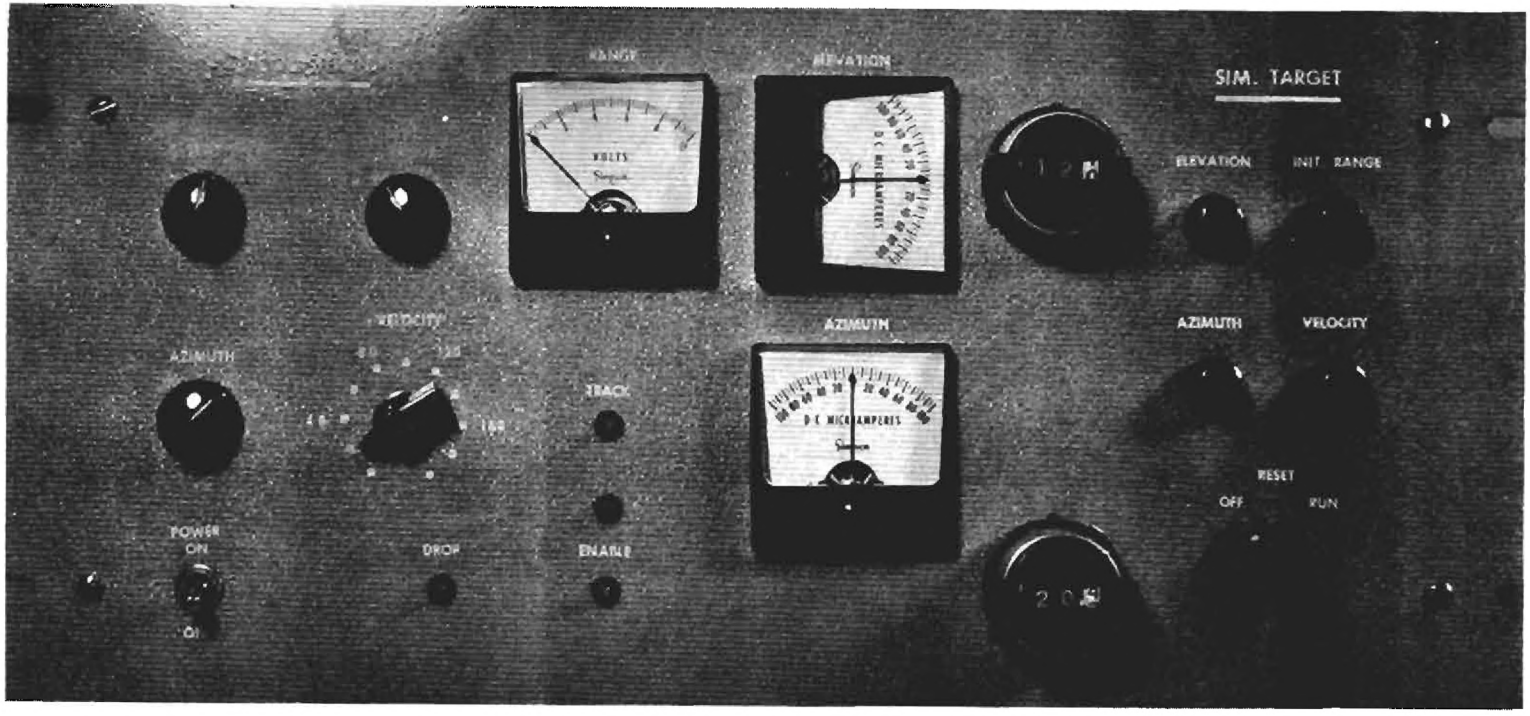


Figure 18. Photograph of Tracking Unit Front Panel Controls.

3.2.8.2 Desired Approach Controls

3.2.8.2.1 Elevation - calibrated potentiometer established desired glideslope. Normally calibrated to read 20 counts per degree, with zero reading corresponding to -1 degree and 220 counts corresponding to +10 degrees.

3.2.8.2.2 Azimuth - calibrated potentiometer establishes desired courseline. Normally calibrated to read 10 counts per degree, with zero reading corresponding to 15 degrees clockwise from scan center and 300 counts corresponding to 15 degrees counter-clockwise from scan center.

3.2.8.3 Simulated Target Controls

3.2.8.3.1 Mode Selection Switch - determines any one of the following states of the simulated target:

1. OFF - no simulated target generated,
2. RESET - simulated target held in initial position determined by simulated target azimuth, elevation, and range controls described below, or
3. RUN - simulated target proceeding from initial state toward radar.

3.2.8.3.2 Elevation - determines elevation angle of simulated target in both RESET and RUN modes. Simulated target proceeds toward radar at a constant elevation angle during RUN, unless this control is moved.

3.2.8.3.3 Azimuth - determines azimuth angle of simulated target in both RESET and RUN modes. Simulated target proceeds toward radar at a constant azimuth angle during RUN, unless this control is moved.

3.2.8.3.3 Range - determines range of simulated target in RESET mode, and initial range in RUN mode. Has no effect on target position if moved during RUN mode, but establishes range to which simulated target returns in RESET mode.

3.2.8.3.4 Velocity - determines velocity of simulated target any any time during RUN mode. Has no effect on target position during RESET, but establishes initial velocity for the next RUN. Simulated target proceeds at constant velocity during RUN mode unless this control is moved.

3.2.8.4 Front Panel Indicators

3.2.8.4.1 Range Meter - indicates range to touchdown of tracking gates while tracking, and range to touchdown of acquisition window when tracking is not in progress. Normally calibrated 0 to 10 nautical miles.

3.2.8.4.2 Elevation Meter - indicates angular difference between elevation tracking gate and desired glidepath. Simulates the elevation pointer of a crosspointer indicator.

3.2.8.4.4 "State Indicator" lights - the amber ENABLE light comes on when the system is able to acquire a target. When a sufficient number of hits have been received in each gate coordinate, the system goes into an Acquisition state indicated by simultaneous operation of the amber ENABLE light and the green TRACK light. If the system remains in the Acquisition state for a sufficient length of time (preselected), the system goes into a track state. This state is indicated by the amber light going out, leaving only the green TRACK light.

3.3 Detailed Circuit Descriptions for Tracking Unit

3.3.1 Conventions and Common Features

3.3.1.1 Input/Output

Input and output signal flow is schematically shown with arrow tails and heads, respectively, with terminal numbers labeled with a "T". Brief word descriptions of the signals are given when necessary.

3.3.1.2 Component Symbols

Standard symbols are used for resistors, capacitors, diodes, transistors, relays, and simple analog integrated circuits such as amplifiers and comparators and digital integrated circuits such as NAND and NOR gates. Pin numbers are shown with the symbol. A very few special integrated circuits are used for simplicity. These are analog switches. Their individual components are shown as discretes; the group is then enclosed with a dashed line and appropriate notation given.

3.3.1.3 Component Identification

Resistors and capacitors in the signal flow path are labeled in close proximity to their symbol with an appropriate prefix and number, as well as their value. Diodes, transistors, and integrated circuits are labeled only with appropriate prefix (D, Q, and IC, respectively) and number, with their normal identification given in one or more notes on the drawing.

Bypass capacitors are identified with special notes and, in some cases, drawings.

3.3.1.4 Junctions

Junctions between two components are clearly labeled with large darkened circles.

3.3.1.5 Waveforms

Liberal use of waveform sketches is made where it was felt they improved clarity. Polarity of DC voltages is given.

3.3.1.6 Test Points

Test points are shown as a line branching from the normal signal path terminated with a large undarkened circle. The test point numbers begin

anew with each board and are labeled with a "TP" prefix. The labels are located next to the circles.

3.3.1.7 Power Supply Bus

Six voltage levels, including ground, are required. Their respective terminals are common for each board. The terminal-voltage correspondence is as follows:

T16 -- +3.6 volts
T17 -- +12 volts
T18 -- -6 volts
T19 -- Ground
T20 -- +15 volts
T21 -- -15 volts

These connections are not shown on the individual diagrams.

3.3.1.8 Test Points

Test points are used to provide access to important waveforms on each board. The numbering of the test points is such that TP1 is the test point closest to the front panel. Test point TP1 is GROUND on all boards.

3.3.2 Board-by-Board Circuit Descriptions

3.3.2.1 Board No. 1 - Input Signal Conditioner - Timing Signals - Figures 19 and 20

The pretrigger, a negative going (from ground) pulse of - volts enters T2 with its coaxial shield entering on T3. The shield is grounded. The pretrigger is terminated by R5. It is then converted to a pulse going negative from +3.6 volts to ground by the C3, R6, D2 combination. This logic level pulse is then inverted in IC4D and triggers the 500 microsecond ONE SHOT circuit composed of IC3B, IC3C, C7, and R7. The ONE SHOT output is differentiated by C8 and R23 and made available at TP2. In parallel, it is differentiated by C9 and R22 and sent out on T4.

The Az-El Gate enters on T10 and is short-circuit protected by R12. It is impedance buffered and voltage translated to logic level by the combination of R13, Q3, R16 and R18. It is then inverted by IC4C and sent out on T6. The output of IC4C is inverted and sent out on T5, as well as made

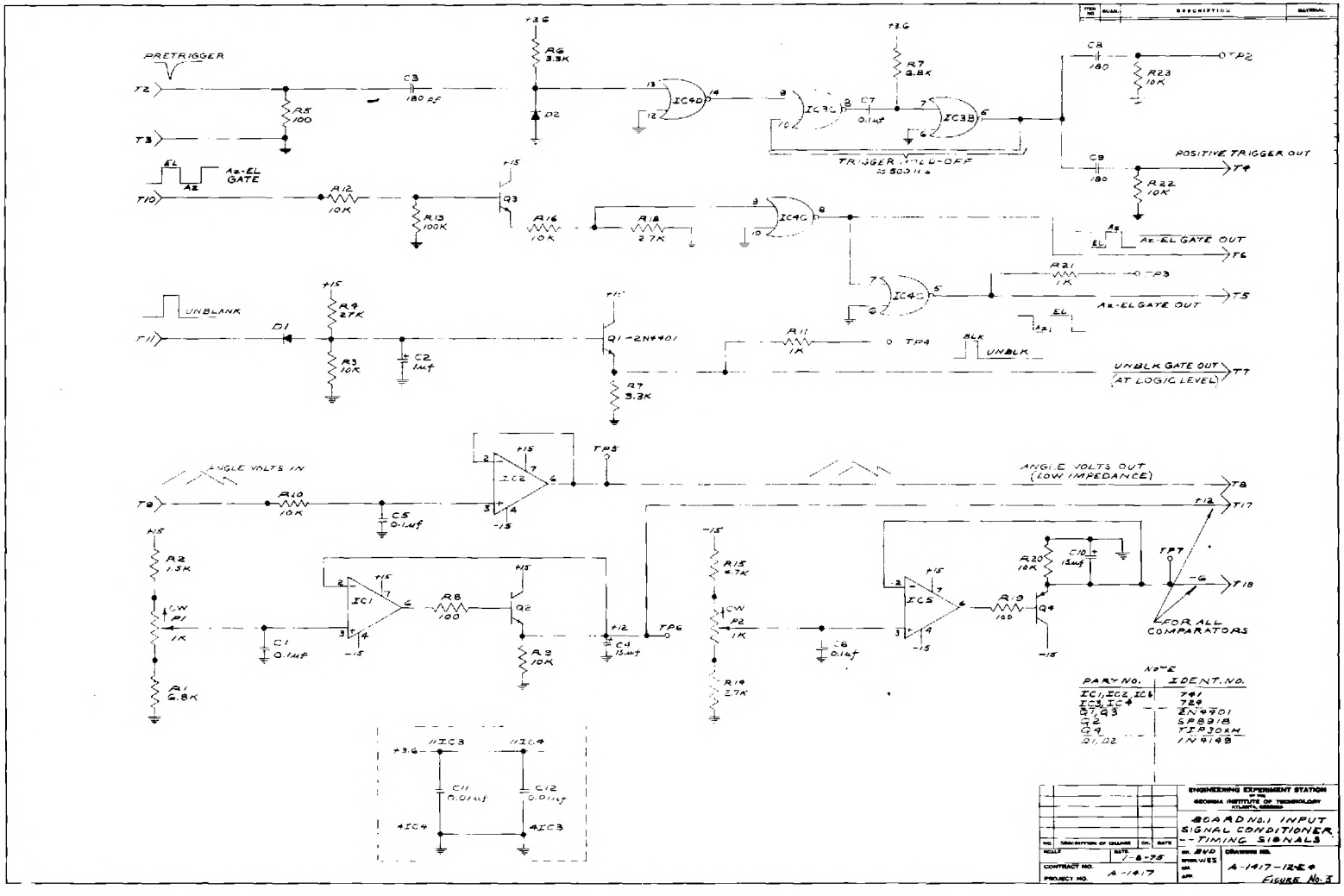


Figure 19. Schematic Diagram of Board No. 1.

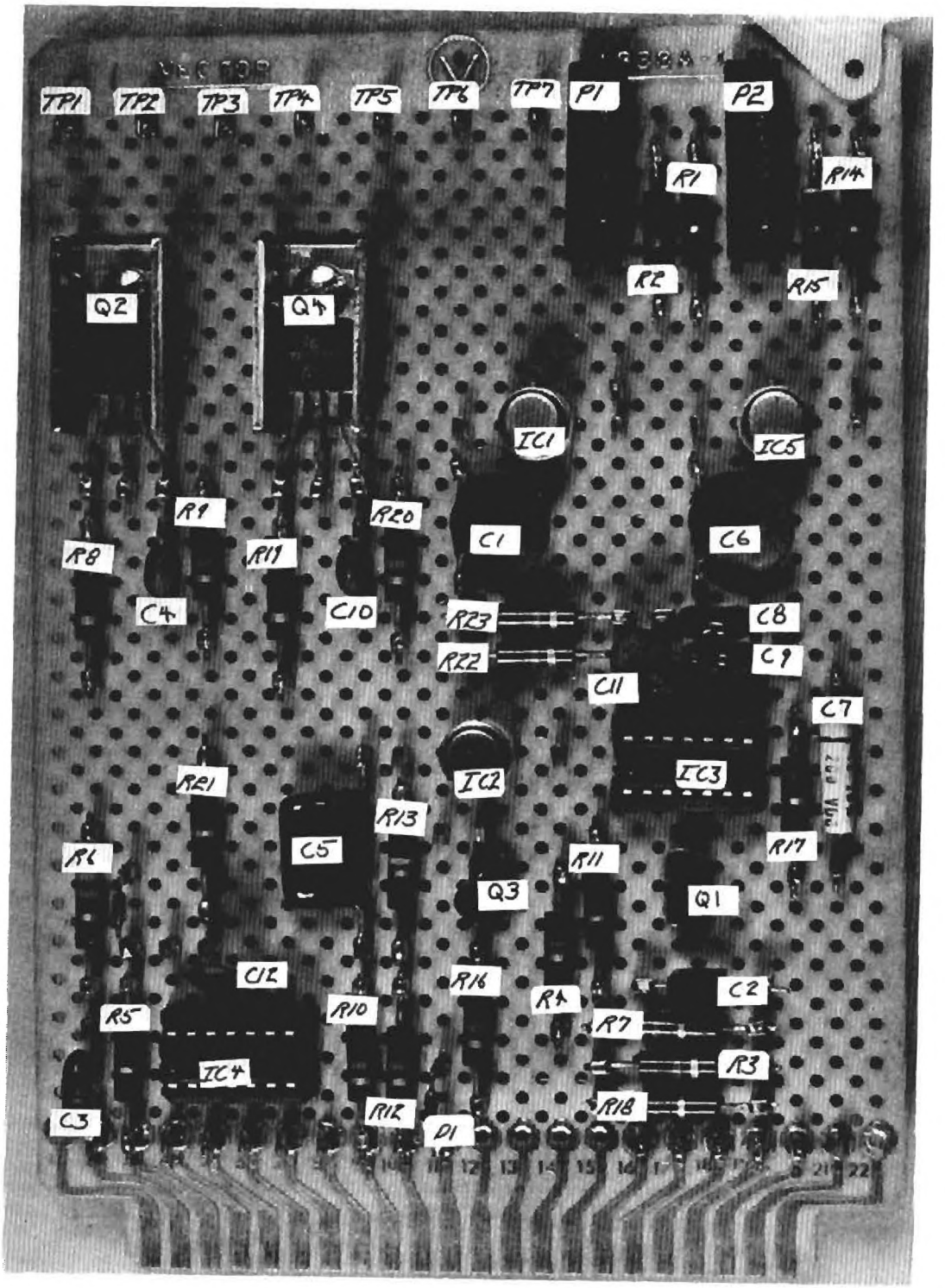


Figure 20. Component Identification Photograph of Board No. 1.

available at TP3 through R21.

The Unblanking signal, a non-positive, bi-level waveform, enters on T11 and is translated to a non-negative, bi-level waveform by the combination of D1, R3, R4, and C2. This signal is impedance buffered by the emitter follower composed of Q1 and R7. The buffered signal is sent out on T7 and also made available at TP4 through R11.

The Angle Volts signal enters on T9, is short-circuit protected by R10, and high frequency bypassed by C5. The signal is then impedance buffered by IC2, made available at TP5, and sent out on T8.

The +12 volt power supply for Boards 2 through 11 is generated on Board 1 as is the -6 volt supply. The +12 volts is obtained by the voltage divider network formed by R1, R2, and P1. Bypass is supplied by C1. A voltage regulator circuit is formed by IC1, R8, R9, Q2, and C4. The regulated +12 volts is sent out on T17 and made available on TP6. The -6 volt circuitry is identical in implementation to that of the +12 volt supply with the components R14, R15, P2, C6, IC5, R19, R20, Q4, and C10 corresponding to R1, R2, P1, C1, IC1, R8, R9, Q2, and C4, respectively. The regulated -6 volts is sent out on T18 and made available at TP7.

3.3.2.2 Board No. 2 - Simulated Target Generator - Figures 21 and 22

The positive trigger enters on T4 and sets a flipflop composed of IC2A and IC2B. When set, the flipflop output goes low, turning off the switch composed of R7 and Q1, allowing C1 to be charged up from the constant current source consisting of R8, R10, and Q2. This ramp voltage is applied to the input resistance R9 and compared to the Simulated Video Range Volts (SVRV) signal in IC6. When the ramp crosses the SVRV signal the output of IC6 goes high. This positive-going edge is differentiated by C3 and R24, as well as being fed back through R23 to reset the flipflop set by the positive trigger. The pulse resulting from the differentiation triggers a ONE SHOT composed of IC7A, IC7B, C4, R25, and P1. The output of the ONE SHOT is a pulse, which serves as the Simulated Video, whose width is set by P1. The Simulated Video is inverted through IC2C and gated by the Az-El Gate in IC2D. From there it is sent out on T2 and made available through R26 at TP3.

The Simulated Target Initial Range voltage (set on the front panel) enters on T10 and is summed directly with a second signal at the output

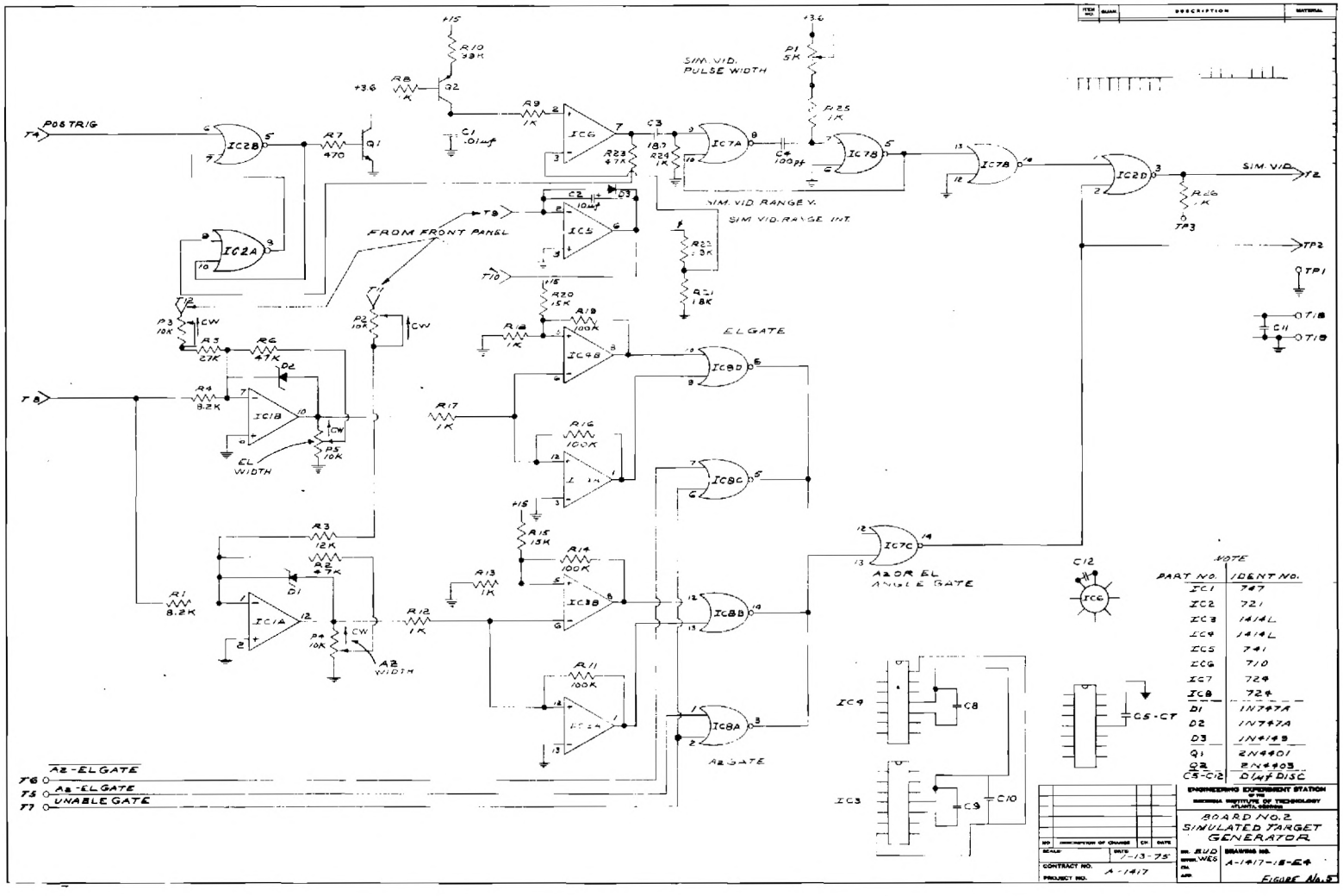


Figure 21. Schematic Diagram of Board No. 2.

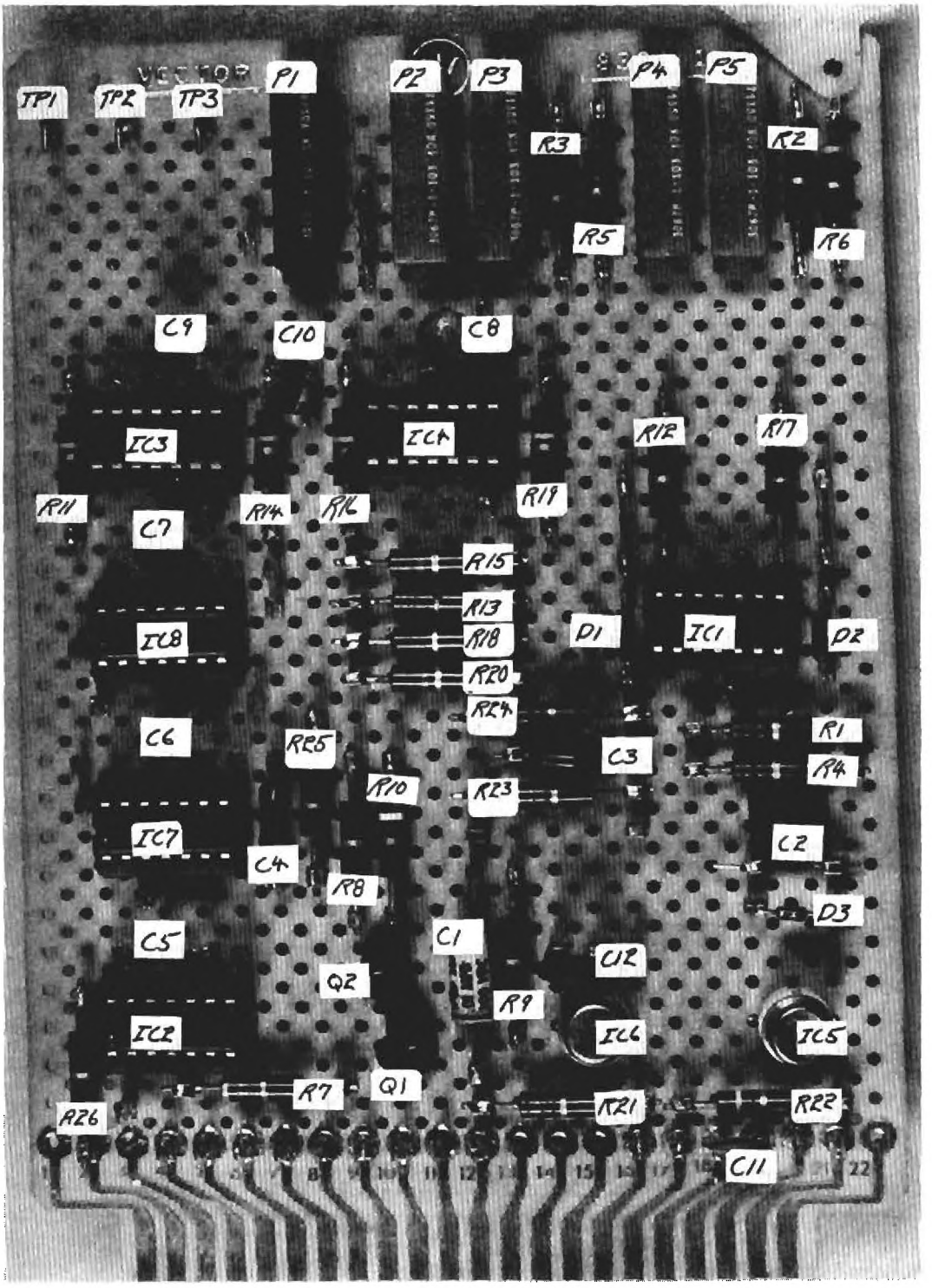


Figure 22. Component Identification Photograph of Board No. 2.

of IC5. This second signal is a negative going ramp derived from the Simulated Target Velocity voltage (also set on the front panel) which enters on T9. The integrator consists of IC5, C2, and D3. The summed voltage is resistive divided by R22 and R21 and becomes the Simulated Video Range Voltage to which the range ramp is compared in IC6.

The Angle Volts signal enters on T8 and simultaneously is differenced in identical circuits to the Simulated Video Azimuth and Elevation Voltages which enter on T11 and T12, respectively, voltages generated on the front panel. The Azimuth difference circuit is composed of R1, R2, R3, P2, P4, D1, and IC1A. The Elevation difference circuit is composed of R4, R5, R6, P3, P5, D2, and IC1B. The differenced outputs are compared simultaneously to GROUND and approximately +1 volt references. When the differenced output passes through this voltage region, the two comparator outputs are low. This condition allows the output of the following two-input gate to go high generating an angle gate. The azimuth comparator and gate circuit consists of R11, R12, R13, R14, R15, IC3A, IC3B, and IC8B. The elevation comparator and gate circuit consists of R16, R17, R18, R19, R20, IC4A, IC4B, and IC8D.

The UNBLANK Gate enters T7, Az-El Gate enters on T5, and the inverse of the Az-El Gate Enters on T6. The UNBLANK Gate gates the Az-El Gate in IC8A and its inverse in IC8C. These resulting gating signals in turn are OR'ed with the Az Gate and the El Gate, respectively. These signals are OR'ed in IC7C whose output gates the simulated Video in IC2D and is made available at TP2.

3.3.2.3 Board No. 3 - Input Signal Conditioner - Video - Figures 23 and 24

The Range Dump signal, a positive pulse, enters on T6 and is gated by the Elevation Gate from T8 and the Azimuth Gate from T7. The gating circuit consists of D1, D2, R4, IC1B, and P4. The use of the Range Dump signal here is to serve as a Range Gate Marker for the indicator; hence it is mixed (added) to the video signal. The screwdriver adjustment, P4, controls the marker amplitude.

The Simulated Video enters on T2 and passes through an amplitude control circuit consisting of R2, R3, IC1A, and P5, a screwdriver adjustment.

The Video signal from the radar receiver enters on T3 and its shield on T4. If the tracking unit is off, the video passes through the normally closed contacts of a relay and is sent out on T5, unmodified. It is also made available through R10 at TP2. If the tracking unit is on, the Video signal is

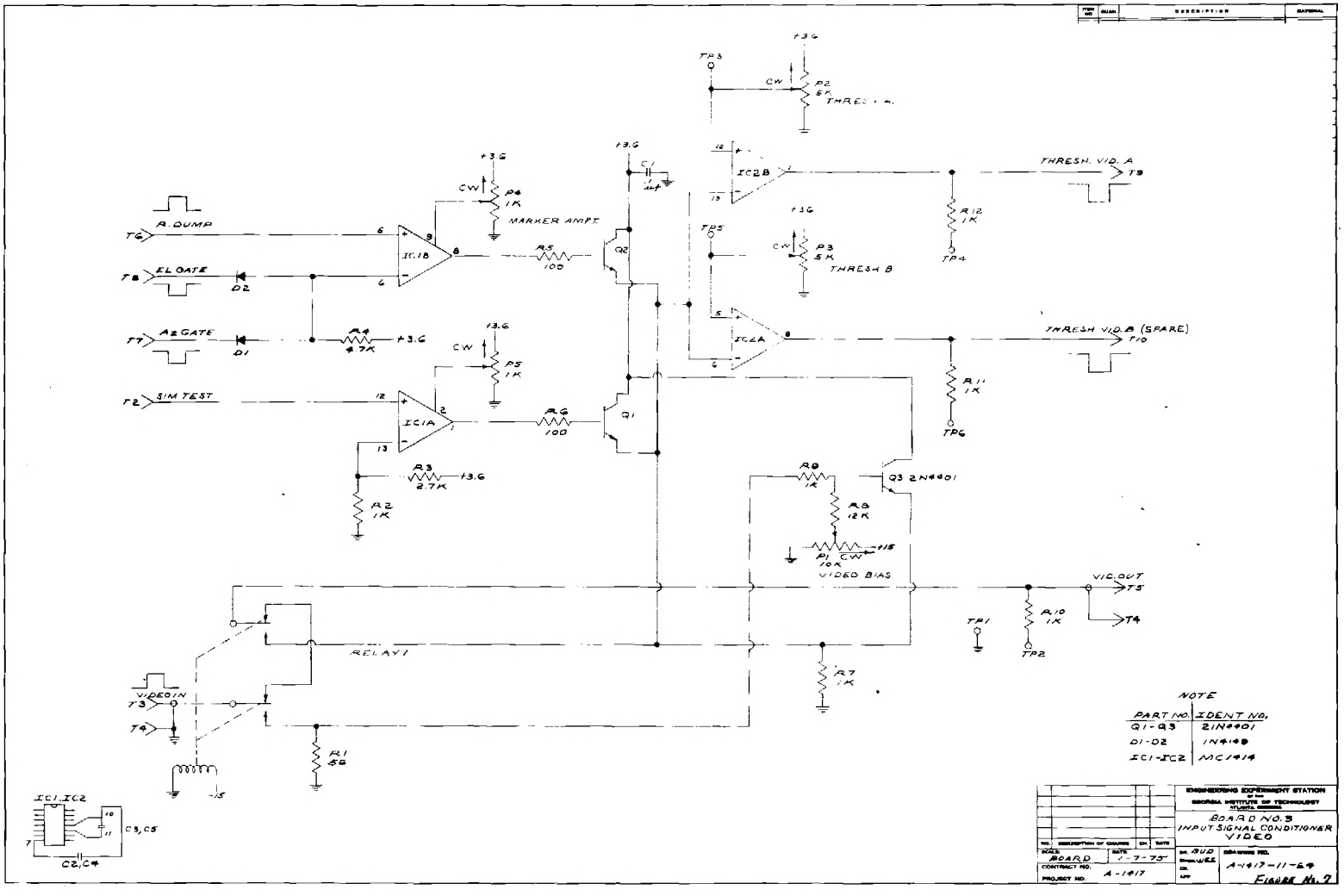


Figure 23. Schematic Diagram of Board No. 3.

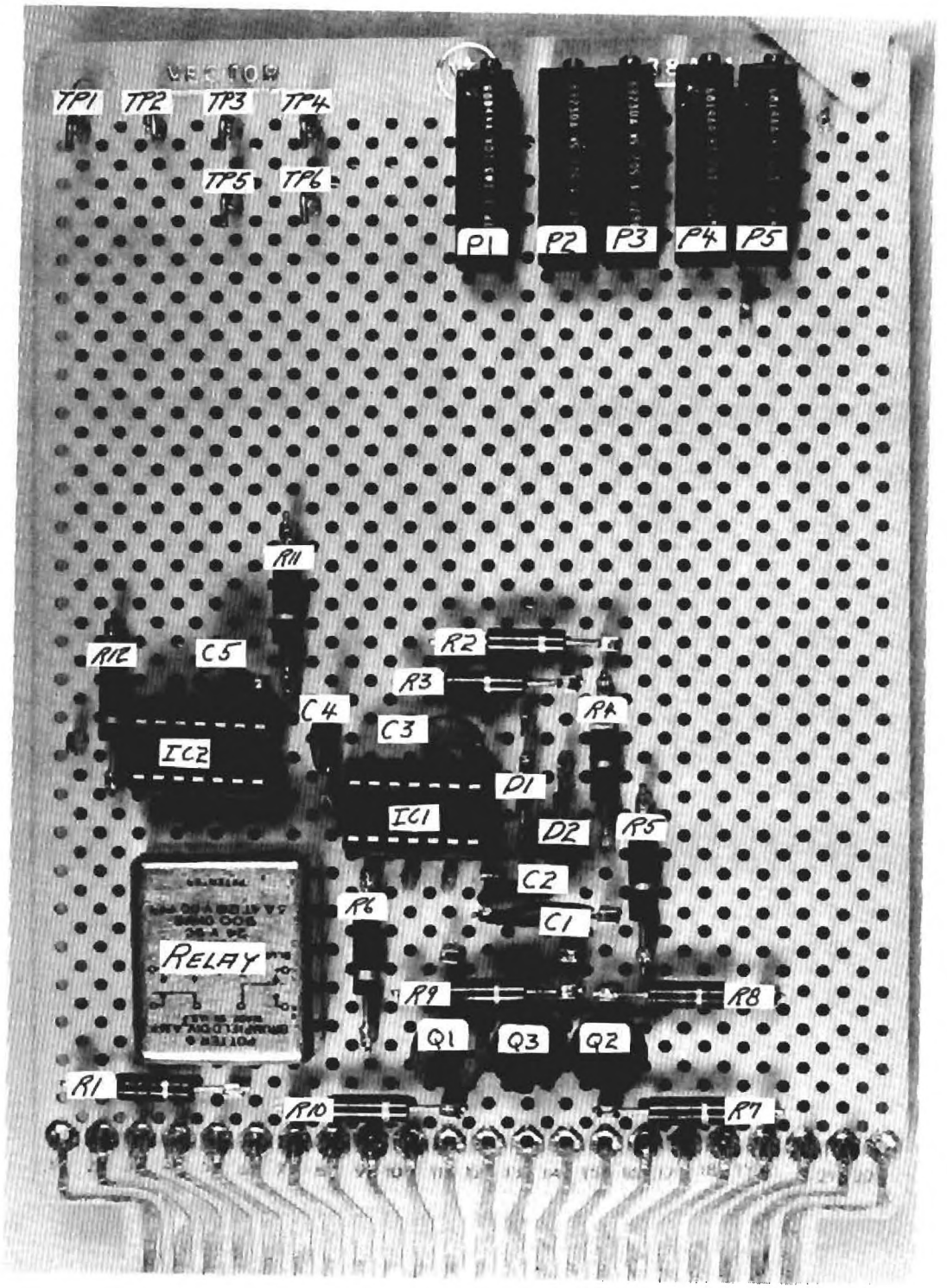


Figure 24. Component Identification Photograph of Board No. 3.

terminated by R1, impedance buffered and biased by R7, R8, R9, P1, and Q3, and added to the Simulated Video and the Range Marker via R5, R6, Q1, and Q2. The summed video signal is compared to Threshold A, a screwdriver adjusted voltage set by P2, in IC2B. Threshold A is made available at TP3. The thresholded video is sent out on T9 and made available through R12 at TP4. The summed video signal is processed by an identical circuit consisting of IC2A, P3, and R11. This threshold is called Threshold B. The output is provided only as a spare, and is not used elsewhere.

3.3.2.4 Board No. 4 - Range Tracker - Gates - Figures 25 and 26

The positive trigger enters on T2 and sets a flipflop consisting of IC1A and IC1B. When set, the flipflop output goes low, cutting off Q1 through R1 and allowing the constant current source of R2, R3, and Q2 to charge C1 at a constant rate. The resulting ramp voltage uniquely relates time delay from the positive trigger to range relative to the radar (with appropriate calibration).

This ramp voltage is compared with a voltage proportional to the Range Volts signal, the current range estimate out of the Range Tracker. The proportionality is obtained through the voltage divider consisting of R4 and R5. The voltage reduction was necessary because of input voltage range restrictions on the comparator, IC2. When the output of IC2 goes high, the output is used to reset the flipflop set by the positive trigger. This turns on Q1 thus discharging C1 causing the output of IC2 to go low again. The time response around this RESET loop is very short, resulting in a short pulse being generated at the output of IC2. This pulse, which is sent out through R7 on T7, is called the Range Trigger.

The Range Trigger pulse is used on this board to perform two functions: (1) generation of the Range Dump pulse which dumps the error sampling circuit on Board 5 and (2) generation of the range gates.

The Range Dump pulse is generated as follows. The Range Trigger pulse, through R6, sets a flipflop composed of IC3C and IC3D. The positive-going edge out of IC3C is the leading edge of the Range Dump pulse sent out on T6. The trailing edge of the pulse occurs when the flipflop is reset by means of a comparator circuit consisting of R29, R30, IC7B, R31, R32, and R8. The Comparator is switched when a fast ramp (described below) crosses a fixed reference voltage. The delay is such that the Range Dump pulse width is approximately 0.6 microseconds.

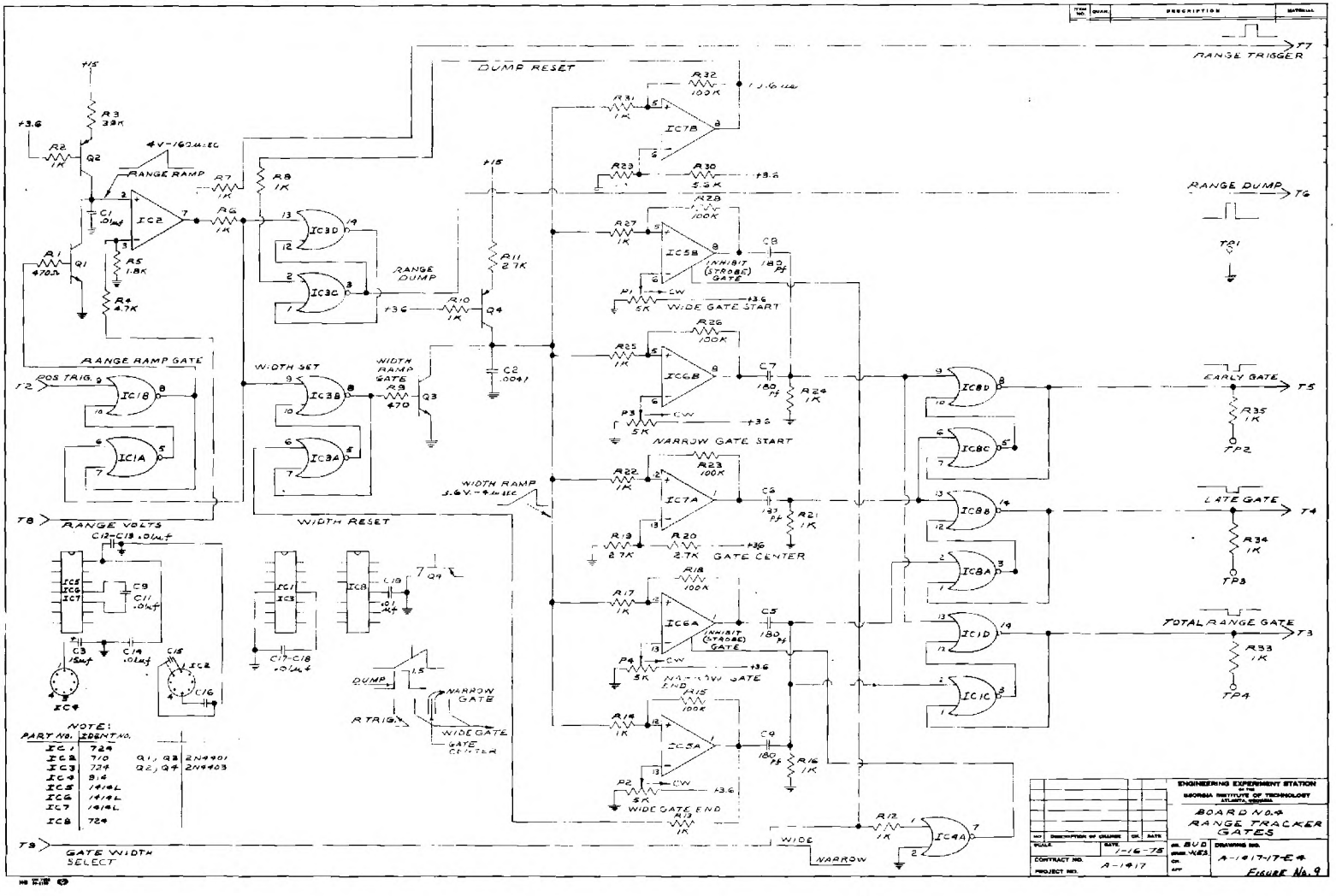


Figure 25. Schematic Diagram of Board No. 4.

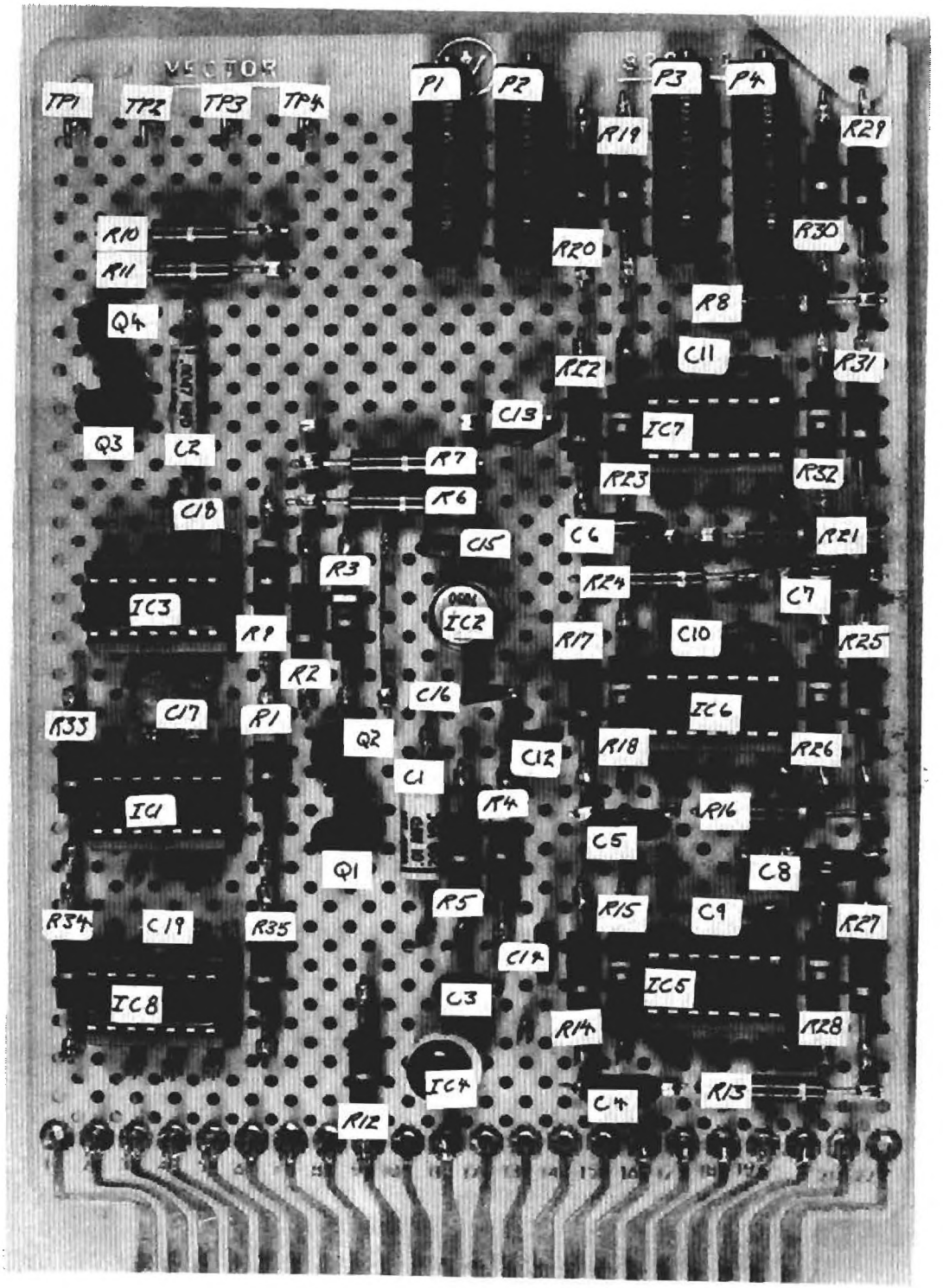


Figure 26. Component Identification Photograph of Board No. 4.

The Range Gates (Early, Late, and Total) are generated as follows. Again the Range Trigger is used to set a flipflop composed of IC3A and IC3B. When set, the output of IC3B goes low and cuts off Q3 through R9. The constant current source consisting of R10, R11, and Q4 then charge C2 producing a steeply rising (0.9 volt/μsec) ramp. The ramp is compared with several reference voltages, one of which was described above to reset the Range Dump flipflop. The five other reference voltages correspond to the following five points in range: (1) the start of the Wide Range Gate (Acquisition Gate), (2) the start of the Narrow Range Gate (Tracking Gate), (3) the center of the Range Gate (both wide and narrow gates are centered at same point), (4) the end of the Narrow Range Gate, and (5) the end of the Wide Range Gate. As the ramp crosses these separate voltages in succession, the respective comparator outputs go high if the comparator is not inhibited. The positive going edge is differentiated, producing short pulses at each of these points in range. The Gate Width Select signal, which enters on T9 and is inverted through R12 in IC4, is used as an inhibit signal (both it and its inverse) to allow only the appropriate pulses through to achieve Wide or Narrow Range Gates.

The width of the Early and Late portions of the Wide or Narrow Gates are controlled by adjusting (screwdriver adjustment) the reference voltages at which the comparator circuit flips. The center of the gates is fixed at approximately a 2 microsecond (≃1.8 volts) delay. The gate controls are as follows:

Wide Gate Start	P1
Wide Gate End	P2
Narrow Gate Start	P3
Narrow Gate End	P4

The Wide Gate End pulse is never inhibited (not necessary due to gating circuitry after comparators) and that output from IC5A is used, through R13, to reset the flipflop which was set by the Range Trigger. When the flipflop is reset, Q3 is turned on and discharges C2. The circuit is then ready to begin another cycle.

The pulses generated by the comparator output transitions are processed in the following manner. The Early Gate, which is sent out on T5 and made available through R35 at TP2, is generated by the setting and resetting of a flipflop consisting of IC8C and IC8D. The flipflop can be set by either the Wide Gate Start pulse or the Narrow Gate Start pulse. If it is set by the Wide

Gate Start pulse, the Narrow Gate Start pulse which occurs shortly thereafter (but before the reset) has no effect. It is reset by the Mid Gate pulse. Therefore, to produce a Narrow Early Gate all that is required is to inhibit the Wide Gate Start Pulse. The Late Gate, which is sent out on T4 and made available through R34 and TP3, is generated by setting and resetting of a flipflop consisting of IC8A and IC8B. The flipflop is set by the Mid Gate pulse. It can be reset by either the Narrow Gate End pulse or the Wide Gate End pulse. If it is reset by the Narrow Gate End pulse, the Wide Gate End pulse which occurs shortly thereafter has no effect. Therefore, to produce a Narrow Late Gate, all that is required is to not inhibit the Narrow Gate End pulse. The Total Range Gate, which is sent out on T3 and made available through R33 at TP4, is generated by setting and resetting a flipflop consisting of IC1C and IC1D. The flipflop is set by either the Wide Gate Start pulse or the Narrow Gate Start pulse and reset by either the Narrow Gate End pulse or the Wide Gate End pulse.

In summary, the Wide Gates (Early, Late, and Total) are generated when the Gate Width Select signal is high such that the Wide Gate Start pulse is not inhibited and the Narrow Gate End pulse is inhibited. When the Gate Width select pulse is low, the opposites are true and Narrow Gates result.

3.3.2.5 Board No. 5 - Range Tracker - Tracking Loop - Figures 27 and 28

The Range Gate signal enters on T3 and gates the Thresholded Video which enters on T12. When the Thresholded Video and Range Gate are present simultaneously, the output of IC2B goes high and sets a flipflop composed of IC2A and IC2C. When set, the output of IC2C goes low and stays in that state until almost a full interpulse interval later when the Range Trigger pulse entering on T7 resets the flipflop. On one angular sweep by the target, with the range gate on the target, the output of IC2C is a binary output which is low almost all of each interpulse period (of which there are many during a single angular sweep across the target). The output is up only for the few microseconds that the Range Trigger precedes the Range Gate. The output of IC2C low-pass filtered with R8 and C2 (to remove these short positive spikes) and sent out on T11 as the Range Gated and Stretched Video, which is also made available at TP5.

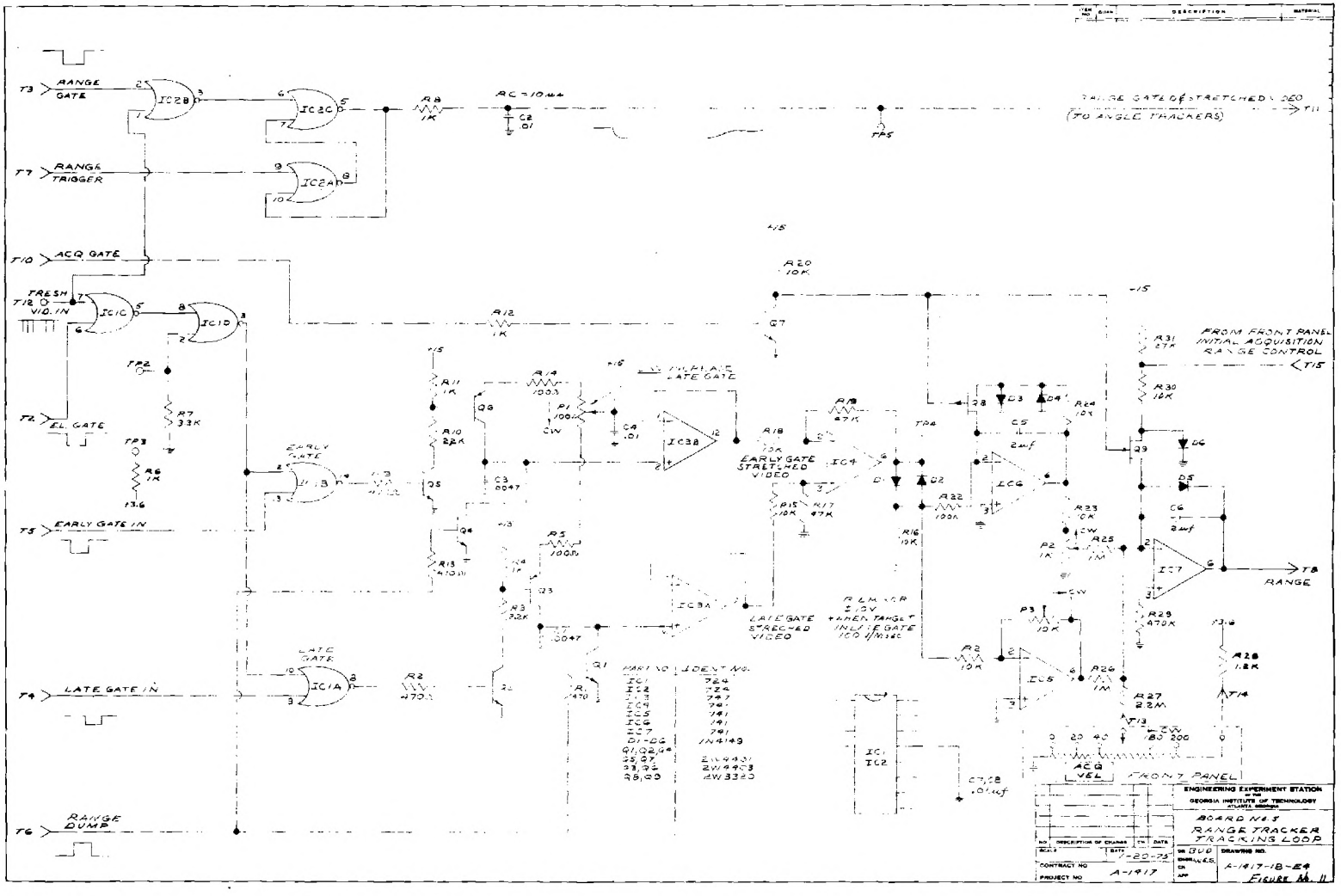


Figure 27. Schematic Diagram of Board No. 5.

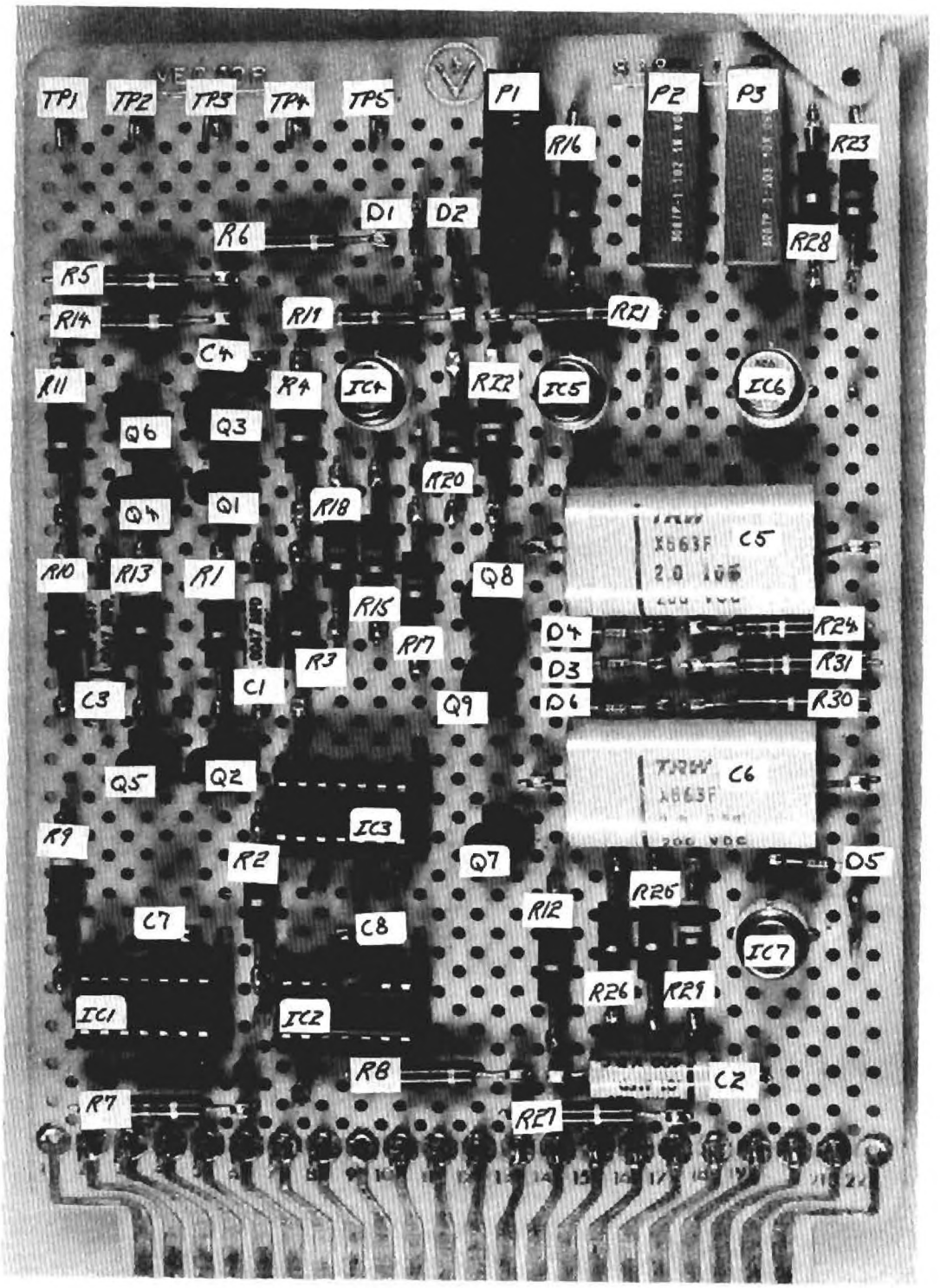


Figure 28. Component Identification Photograph of Board No. 5.

The Elevation Gate enters on T2 and gates the Thresholded Video in IC1C. This gating has inverted the Thresholded Video, so it is again inverted in IC1C. The other input to IC1D is tied to TP2 across R7 to GROUND. The 3.6 volt supply is also brought out through R6 to TP3. The test points TP2 and TP3 may be tied together to simulate thresholded video at all angles. This provision is helpful in the alignment procedures.

The Acquisition Gate enters on T10 and, when high, turns on Q7 through R12, tying one end of R20 essentially to ground (saturation voltage of Q7). This action lets current flow through Q8 and Q9, which in turn clamps to zero the first integrator in the loop and clamps to the Initial Acquisition Range voltage the second integrator in the loop. When the Acquisition Gate is low, Q8 and Q9 are turned off and the integrators are free to act on their incoming signals. The Range Track function can then be performed.

The thresholded and elevation gated video out of IC1D is inputted to IC1A and IC1B in which it is gated through by the Late Range Gate and Early Range Gate, respectively. The outputs of these gates are passed through R2 and R9, respectively, and turn on Q2 and Q5, respectively. Turning on Q2 appropriate bias due to R3 and R4 to be applied to Q3 to turn it on. A constant current source is formed by Q3, R5, and some portion of P1, which charges up C1 by an amount directly proportional to the fraction of the thresholded video pulse was in the late gate. Turning on Q5 performs the same operation for the Early Gate through R10, R11, Q6, R14, and the rest of P1. The charging capacitor for the Early Gate is C3. The charging circuits are intended to be identical; any differences are balanced out by P1. The voltages on C1 and C3 are impedance buffered by IC3A and IC3B, respectively, and differenced in IC4 with balanced gains provided by R15, R17, R18, and R19. The output of IC4 is the Range Error voltage which the Tracking Loop acts to drive to zero.

The charging capacitors, C1 and C3, must be dumped each interpulse period just before the next sample. This dumping is accomplished by the Range Dump pulse which enters on T6 and turns on Q1 and Q4 through R2 and R13, respectively.

During normal tracking, the Range Error Voltage at the output of IC4 is inputted an integrator circuit composed of R22, C5, IC6, R23, and P2 and an amplifier circuit composed of R21, IC5, and P3. The outputs of IC5 and IC6 (through R23, P3 voltage divider) are summed through R26 and R25, respectively,

with the Acquisition Velocity voltage from the front panel through R26. The summed voltage is integrated by IC7 and C6 to produce the Range Volts (tracker estimate of target range) signal which is sent out on T8. In normal operation the Range Error signal out of IC4 has magnitude of significance only during the portion of the elevation sweep when the elevation beam passes across the target. Otherwise, the output of IC4 is near zero except for amplifier drift. Diodes D1 and D2 are used to prevent small signal drift from being integrated in IC6 between elevation scans across the target. During these intervals the loop is essentially tied to GROUND through R16 and is operating as an open loop.

3.3.2.6 Boards 6 and 8 - Angle Tracker - Gates - Figures 29 and 30

Boards 6 and 8 are component-by-component identical, differing only, and not necessarily, in potentiometer settings.

The Angle Volts signal enters on T7 and is resistively summed via R1 and R3 with the Angle Track Volts signal entering on T12. Since the Angle Volts signal is strictly negative and the Angle Track Volts signal is strictly positive, their sum can be positive or negative depending on relative magnitudes. When the Angle Volts signal is equal in magnitude to the Angle Track voltage, their sum equals zero and this corresponds to the antenna beam pointing in the direction of the center of the Angle Tracking Gate.

As the Angle Volts signal sweeps by the Angle Track Volts signal (in magnitude) the output of the amplifier IC1 is swept through its output voltage range which is limited by the zener diodes, D1 and D2, to be from -3.6 volts to +3.6 volts. How fast the output traverses its output depends on its gain, which in turn is selected through switching circuitry by the Gate Width Select signal entering on T8. Since the output of IC1 is compared to fixed reference voltages of approximately -1 volt, 0 volts, and +1 volts to obtain, respectively, the "minus" angle gate and "plus" angle gate, it follows that the more quickly the transitioning between the references occurs, the narrower the gates. Therefore, higher feedback gain around IC1 produces a narrower gate. Gate width adjustments are obtained with P1 and P2 (screwdriver adjustments).

The Gate Width Select signal enters on T8 and, when high, turns on Q1 through R2. The collector of Q1 is tied to +15 volts through R4 and to the base of Q2 through R5. When Q1 is on, Q2 is off which turns on Q4 and turns

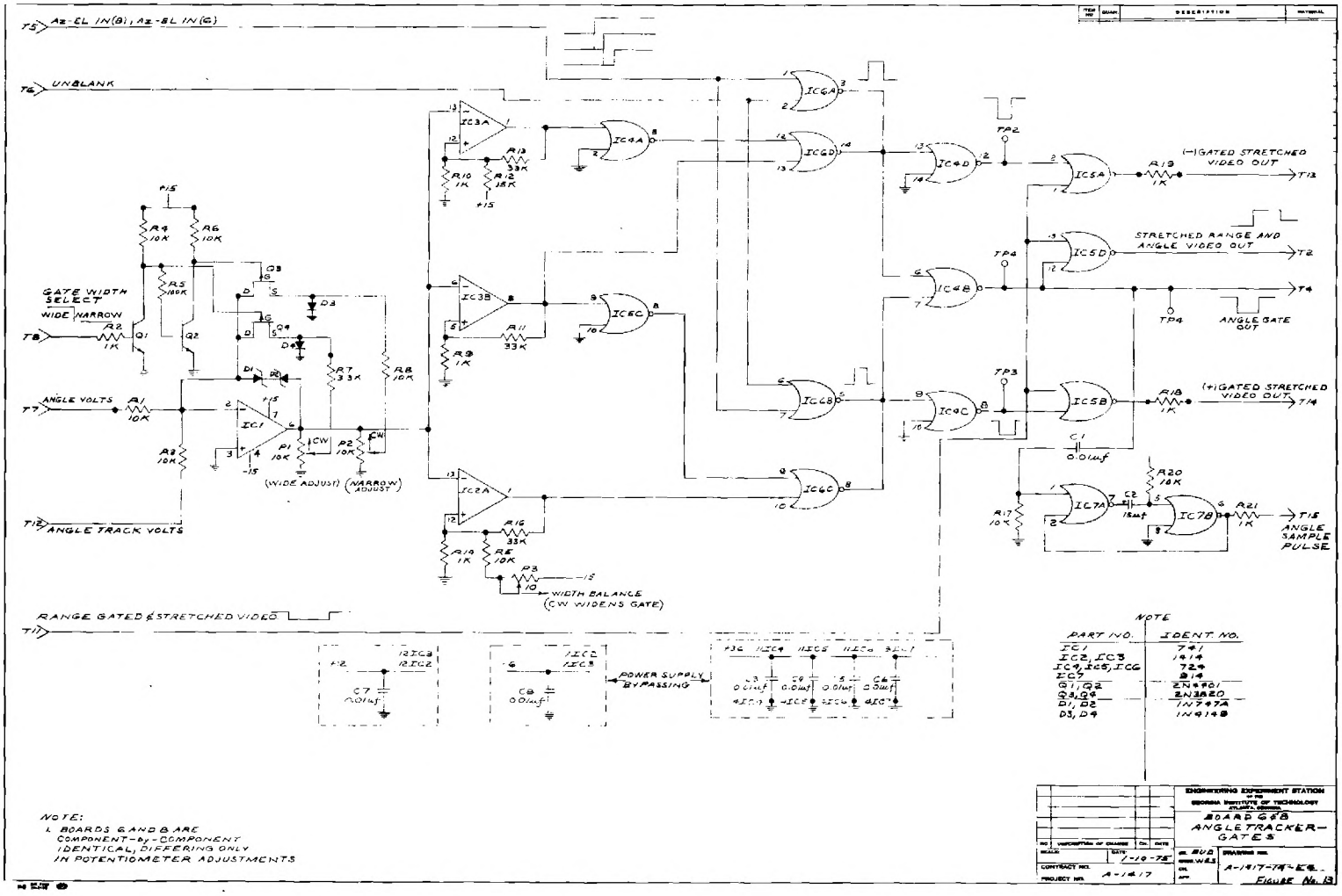


Figure 29. Schematic Diagram of Boards Nos. 6 and 8.

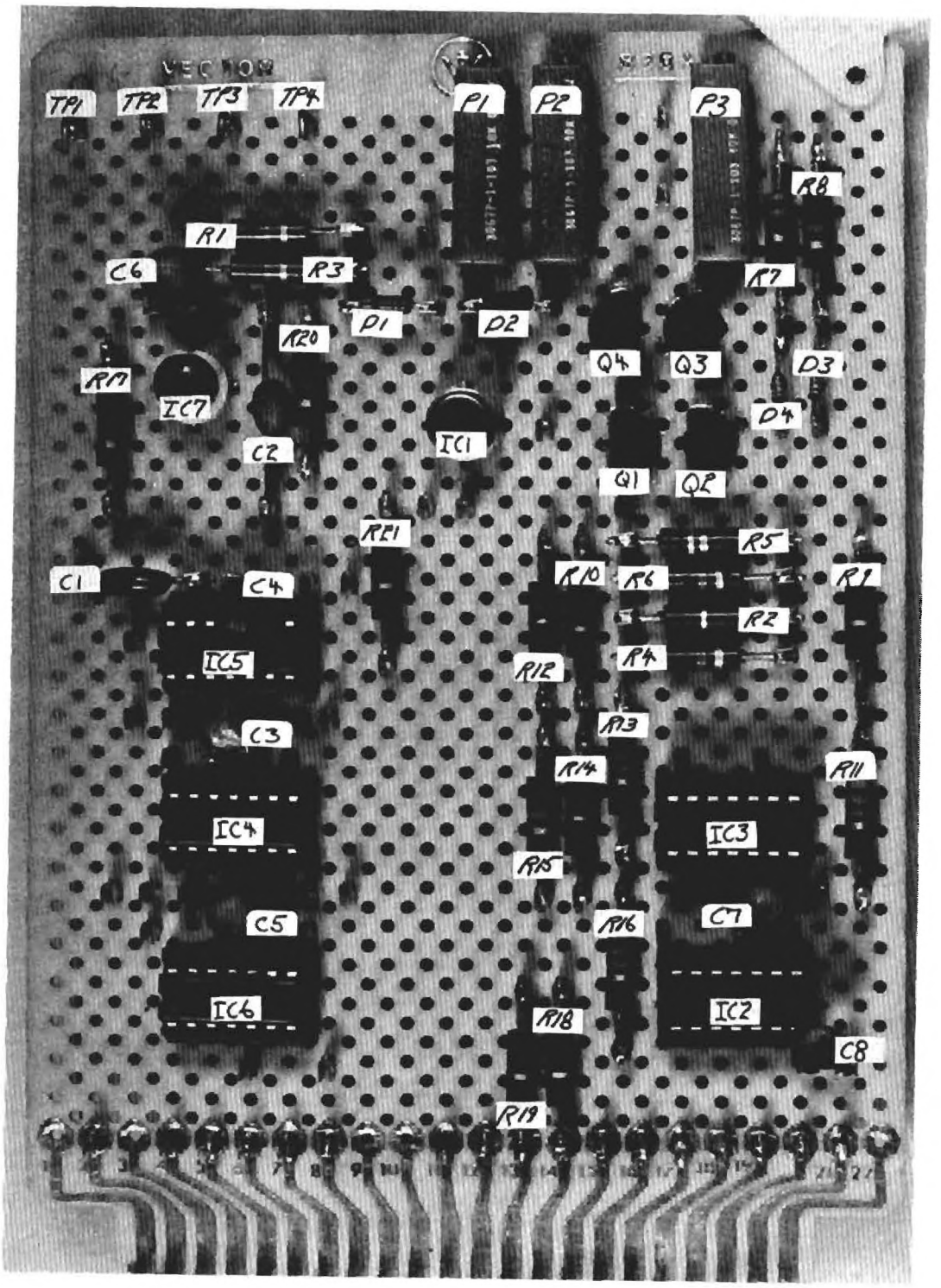


Figure 30. Component Identification Photographs of Boards Nos. 6 and 8.

off Q3, thus connecting R7 as the feedback resistor and choosing the lower feedback gain. When the Gate Width Select signal is low, the opposite conditions exist and R8 is selected as the feedback resistor.

The Angle Gates (Plus, Minus, and Total) are generated by comparing the output of IC1 to fixed reference voltages as described above. Since both antennas (Azimuth and Elevation) make bidirectional passes across the target, the nomenclature of "early" and "late" gates does not apply. The terms "plus" and "minus" were chosen as being somewhat more descriptive. The -1 volt reference circuit is composed of R14, R5, R16, P3, and IC2A. The GROUND reference circuit is composed of R9, R11, and IC3B. The +1 volt reference circuit is composed of R10, R12, R13, and IC3A.

The output of IC2A is inputted to IC6C with the inverted output of IC3B. When the output of IC1 is between -1 volt and GROUND, these two inputs are low producing a high output on IC6B. When the output of IC1 is between 0 volts and +1 volt, the output of IC3B and the inverted output of IC3A are low and produce a high output from IC6D. The outputs of IC6C and IC6D are AND'ed with the outputs, respectively, of IC6B and IC6A, which are produced by simultaneous low inputs from the Unblank signal entering on T6 and the Az-El Gate signal entering on T5. When everything is synchronized properly these signals should always be such that the Plus and Minus Gates are passed.

The Plus Gate and Minus Gate are then inverted in IC4C and IC4D, respectively, as well as inputted to IC4B to produce the Total Gate. The Plus Gate, Minus Gate, and Total Gate are then made available at TP3, TP2, and TP4, respectively. The Range Gated and Stretched Video enters on T11 and is gated by the Plus Gate, Minus Gate, and Total Gate through IC5B, IC5A, and IC5D, respectively. The Plus Gated-Range Gated and stretched Video is sent out on T14 through R18. The Minus Gated-Range Gated and Stretched Video is sent out on T13 through R19. The Total Gated-Range Gated and Stretched Video is sent out on T2. The Total Gate is sent out on T4 and made available at TP4. The total gate is also differentiated by C1 and R17 and used to trigger a ONE SHOT composed of IC7A, IC7B, R20, and C2. The output of the ONE SHOT is the Angle Sample Pulse and is sent out on T15 through R21.

3.3.2.7 Boards 7 and 9 - Angle Tracker - Tracking Loop - Figures 31 and 32

Boards 7 and 9 are component-by component identical, differing only in loop gain potentiometer settings.

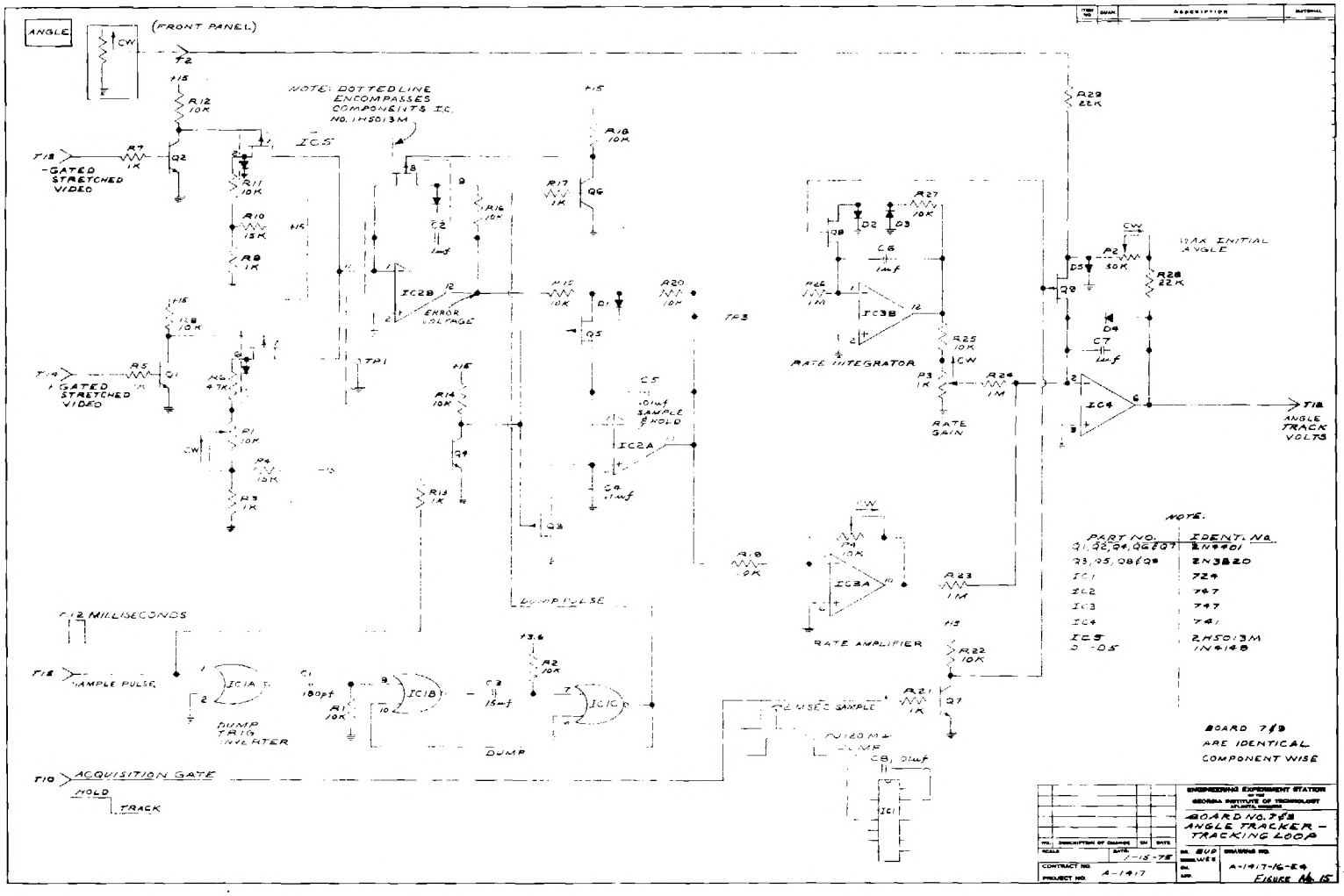


Figure 31. Schematic Diagrams of Boards Nos. 7 and 9.

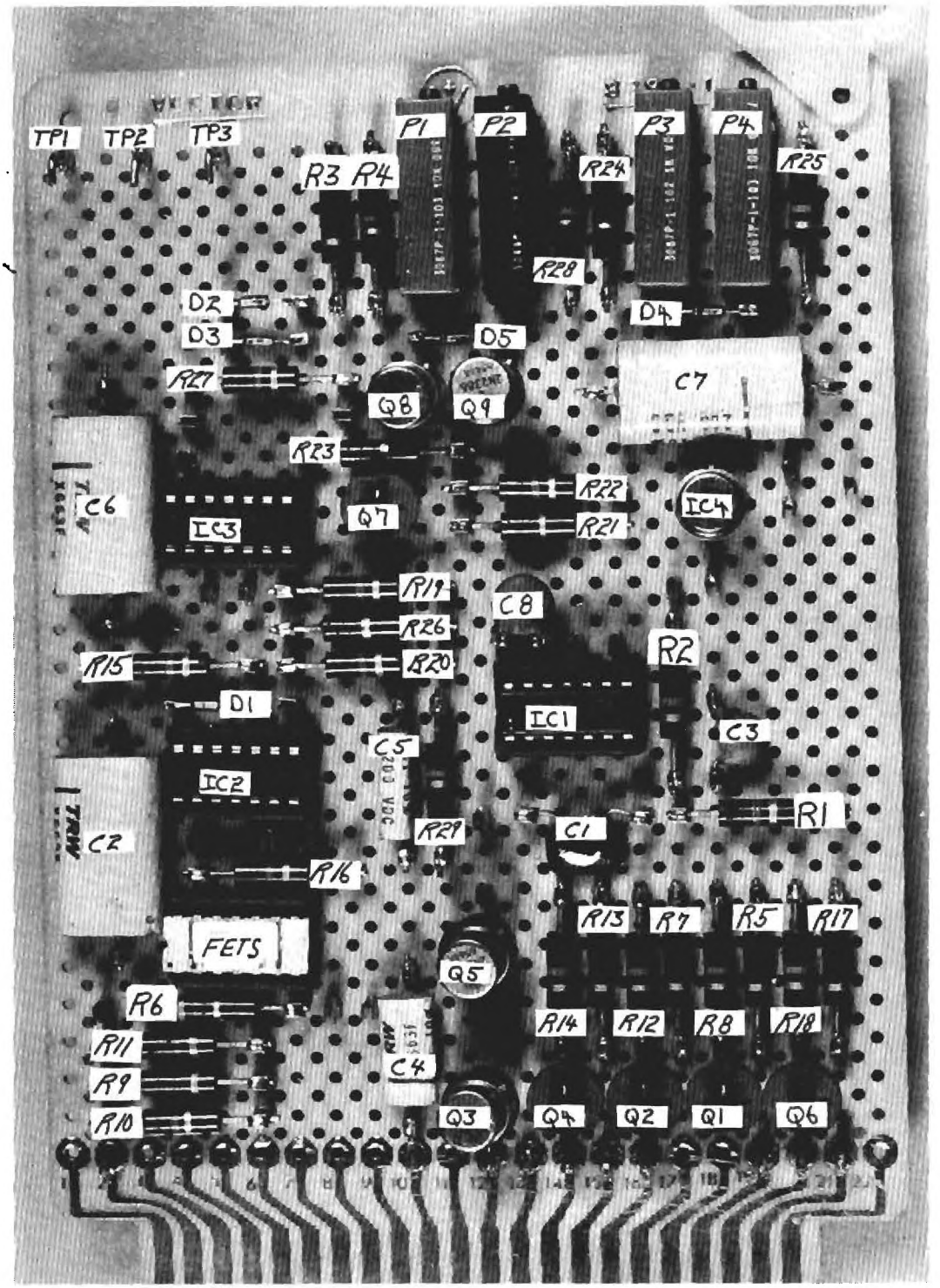


Figure 32. Component Identification Photographs of Boards Nos. 7 and 9.

The Minus Gate-Range Gated and Stretched Video enters on T13. When positive, it turns on Q2 through R7, bringing the collector junction with R12 near GROUND and turning on one of the FET switches in IC5. This allows the approximate +1 volt DC voltage at the junction of R9 and R10 to be an input to IC2B through R11. This voltage is integrated by C2 across IC2B and appears as a positive ramp which increases as long as there is video in the Minus Gate.

As the Minus Gate ends the Plus Gate-Range Gated and Stretched Video enters on T14, turning on Q1 through R5. The collector of Q1 goes low, turning on another FET switch in IC5 which allows the -1 volt DC voltage at the junction of R3 and R4 to be an input to IC2B through P1 and R6. This voltage is integrated by C2 across IC2B and appears as a negative ramp beginning from where the positive ramp from the Minus Gate ended. With equal video in each gate, the integrator output ramps up and then down by dqual amounts, leaving zero resultant error to be sampled by the Sample-and-Hold circuit.

The Sample Pulse enters on T15 and turns on Q4 through R13, bringing the junction between the collector of Q4 and R14 near GROUND and turning on Q3 and Q5. The switch Q3 dumps any residual voltage from the stabilizer capacitor C4. The switch Q5 makes IC2A a unity gain amplifier by placing R20 across C5 with R15 as an input resistance. The output of IC2A, which is made available at TP3, is at that time forced equal to the error voltage output of IC2B. When the sample pulse ends, Q3 and Q5 are opened and C5 holds the error voltage which has just been sampled.

The Dumping operation is implemented as follows. The Sample Pulse is inverted in IC1A and differentiated by R1 and C1. The trailing edge of the inverted Sample Pulse triggers a ONE SHOT consisting of IC1B, IC1C, R2, and C3. When triggered, the output of the ONE SHOT turns on Q6 through R17, bringing the collector junction with R18 low and turning on the third FET switch in IC5 which discharges the Error Voltage across C2, completing the Dumping cycle.

The sampled and held error voltage out of IC2A is parallel processed by an integrator consisting of IC3B, R26, and C6 and an amplifier consisting of IC3A, R19, and P4. The integrator output is voltage divided by R25 and P3. This voltage and the amplifier output are summed by R23 and R24 at the input to a second integrator, consisting of IC4 and C7. This integrator output is the Angle Track Volts signal and is sent out on T12.

The Acquisition Gate enters on T10 and, when high, turns on Q7 through R21. The collector junction with R22 goes low, turning on Q8 which discharges C6 through R27 and D2 or D3, depending on whether the voltage on IC3 is positive or negative, respectively. The collector of Q7 going low also turns on Q9 which transforms the IC4-C7 integrator circuit into an amplifier consisting of IC4, R28, P2, and R29. The input to this amplifier is the Initial Acquisition Angle signal determined by a Front Panel potentiometer setting. The Initial Acquisition Angle signal enters on T2.

3.3.2.8 Board 10 - Automatic Acquisition - Figures 33 and 34

The Range and Elevation Gated and Stretched Video signal enters on T3 and is differenced with the HITS TO ACQUIRE voltage reference (screwdriver adjustable, P1). The difference is integrated in a circuit consisting of R5, C4, IC3B, and D3. The zener diode keeps the input to IC4B from being too large. The output of IC3B is made available at TP3. It is simultaneously impedance buffered and translated to logic levels by the circuit consisting of R6, IC4B, and D4. When it goes positive, the output of IC4B sets a flipflop consisting of IC2C and IC2D. The flipflop is reset by a pulse coinciding with the beginning of the Elevation Gate which enters on T5. The pulse is generated by inverting the Elevation Gate in IC1B and differentiating with R4 and C3. The flipflop output from IC2D is then a bi-level signal which is forced low by the presence of a preset (HITS TO ACQUIRE) number of video pulses within the current elevation scan and forced high again by the beginning of the following elevation sweep across the target.

Identical processing is used on the Range and Azimuth Gated and Stretched Video which enters on T2 and the Azimuth Gate which enters on T4. The resulting bilevel signal appears at the output of IC2B.

The outputs of IC2D and IC2B are inputs to IC1D whose output goes high only when both inputs are low. In other words the logic level signal out of IC1D, labeled ACQ, is high only when a preset number of threshold exceeding video pulses have occurred consecutively in successive sweeps of azimuth and elevation across the target. Either sweep can occur first. Therefore, when ACQ is high, the system should be allowed to begin its tracking function.

The ACQ signal is summed through R9 and D5 with a small negative voltage obtained with R14 and R15 and through R13. The resultant is integrated

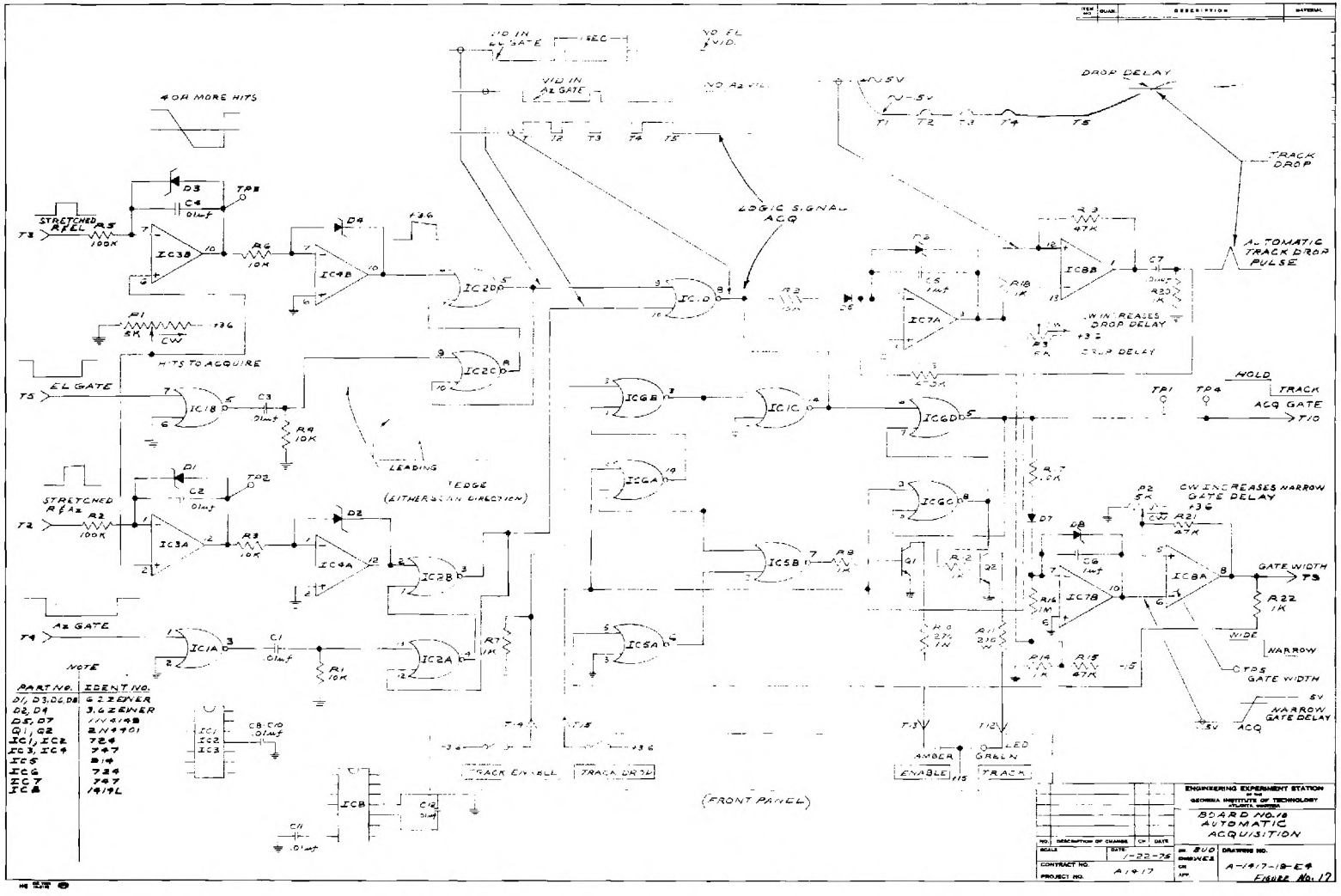


Figure 33. Schematic Diagram of Board No. 10.

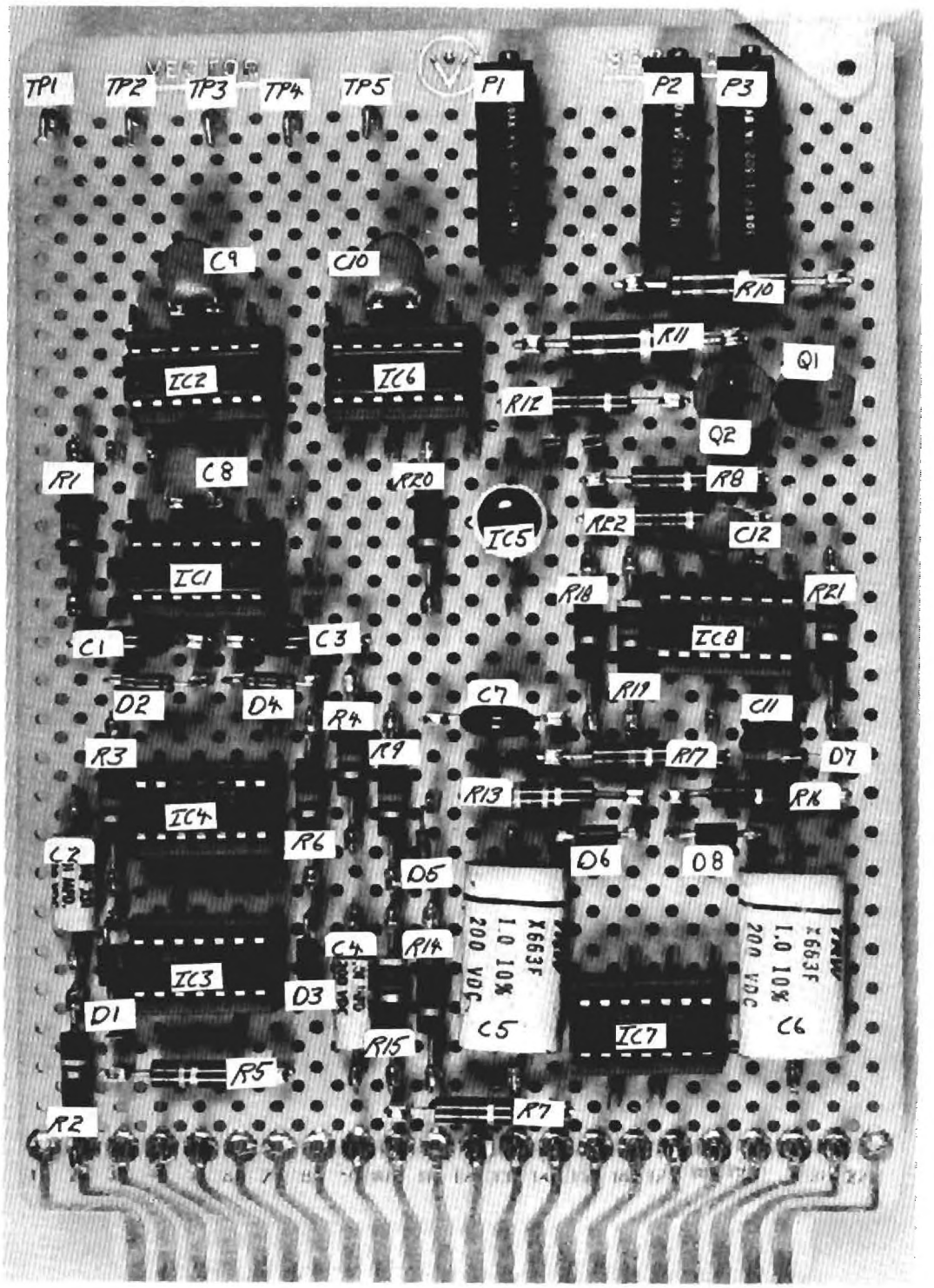


Figure 34. Component Identification Photograph of Board No. 10.

by IC7A and C5. The output is limited between approximately +6 volts and -0.5 volts by D6. When ACQ goes high, the integrator output ramps down at a rate determined by R9 and C5. When ACQ goes low D5 disconnects it from the summing junction and the integrator output ramps up at a rate (much slower) determined by R13 and C5. The output from the integrator is compared to the Drop Delay Reference Voltage set by P3 by a comparator circuit consisting of R18, R19, and IC8B. The output of the comparator is differentiated by C7 and R20 to produce the Automatic Track Drop Pulse used to force the system out of the tracking sequence.

A +3.6 volt signal enters on T14 when the front panel ENABLE button is depressed. The voltage appears across R7. This positive voltage sets a flipflop composed of IC6A and IC6B. When set, the flipflop output from IC6B goes low, is inverted in IC1C, allowing this output to be high. This output is tied directly to ACQ. When this output is high, ACQ is allowed to be high (implying "acquisition" conditions have been met) and a flipflop composed of IC6C and IC6D is set. The output of IC6D is the Acquisition Gate which is sent out on T10. The system is allowed to track its inputs from the radar when the Acquisition Gate is low. The Acquisition Gate is made available at TP4.

As with the ACQ signal, the Acquisition Gate is summed with the small negative voltage via R17 and D7. The voltage formed with R14 and R15 is summed with the Acquisition Gate through R16. The resultant is integrated by IC7B and C6. The output is limited between +6 and -.5 volts by D8. When the Acquisition Gate is high, the integrator output ramps down at a rate determined by R17 and C6. When the Acquisition Gate goes low (indicating "acquisition" conditions exist) the integrator output ramps up at a rate determined by R16 and C6. The integrator output is compared to the Wide-to-Narrow Transition Reference Voltage set by P2 in a comparator circuit consisting of P2, R21, and IC8A. The inhibit input to IC8A is made available at TP5 for alignment purposes. The output from the comparator is the Gate Width Select signal (high corresponds to Wide Gates, low corresponds to Narrow Gates) and is sent out on T9. It is also used through R22, IC5A, IC5B, and R8 to turn off Q1. This action stops current flowing through the series combination of R10 and the amber ENABLE light on the front panel.

A +3.6 volt signal enters on T15 when the front panel DROP button is depressed. This positive voltage resets the flipflop set by depressing the ENABLE button. It also resets the flipflop set by the ACQ signal, forcing the tracking sequence to end. These same two flipflops also can be reset by the Automatic Track Drop Pulse described earlier.

The flipflop which is set by the ACQ signal also serves to control the green TRACK light on the front panel by turning on and off Q2 through R12. The sequence of lights is as follows. When the DROP button has been depressed or Automatic Drop has occurred, both lights are off. When the ENABLE button has been depressed but no target has been acquired (Acquisition Gate is high) the amber ENABLE light only is on. When a target has been acquired but the tracking gates have not narrowed down, both the amber ENABLE light and the green TRACK LIGHT are on. When a target is being tracked with narrow gates, only the green light is on.

3.3.2.9 Board 11 - Output Signal Conditioner - Figures 35 and 36

The Range Volts signal enters on T8 and is differenced with the Range Zero Reference Voltage set by P1. The differencing circuit consists of R16, R17, P1, and IC4A. The output of IC4A is then impedance buffered and amplified in a circuit consisting of R18, R19, P2, D5, and IC4B. The zener diode D5 restricts the output of IC4B to between approximately +12 volts and -0.5 volts. The output of IC4B is the Range to Interface signal and is sent out on T13.

The Elevation Volts signal enters on T11 and is summed with the Elevation Reference Voltage set by a 10-turn, readout type potentiometer on the front panel. The potentiometer ends enter through T4 and T5. The potentiometer acts as a feedback gain around an amplifier consisting of IC2B, R9, and P5. The potentiometer P5 serves as a calibration for the readout potentiometer. The summation is accomplished with R10 and R11. The sum is amplified by the combination of IC5A, R12, and P6. The output of IC5A is impedance buffered and further amplified by the circuit consisting of R13, R14, and IC5B. The zener diodes D3 and D4 restrict the output of IC5B to between +12 volts and -12 volts. The output of IC5B is the Elevation to Interface signal, is sent out on T15 and also on T7 through R15 to the front panel elevation meter.

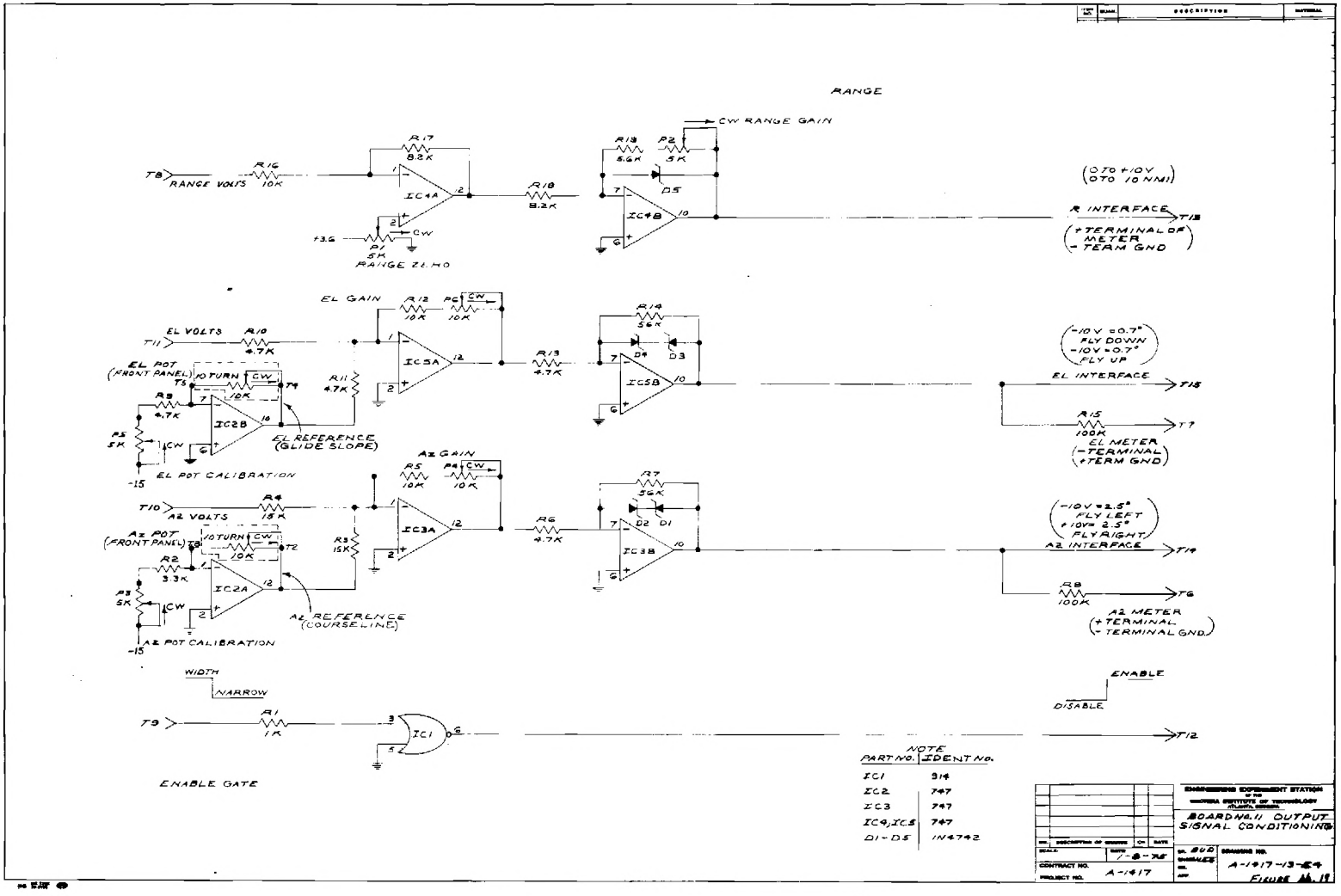


Figure 35. Schematic Diagram of Board No. 11.

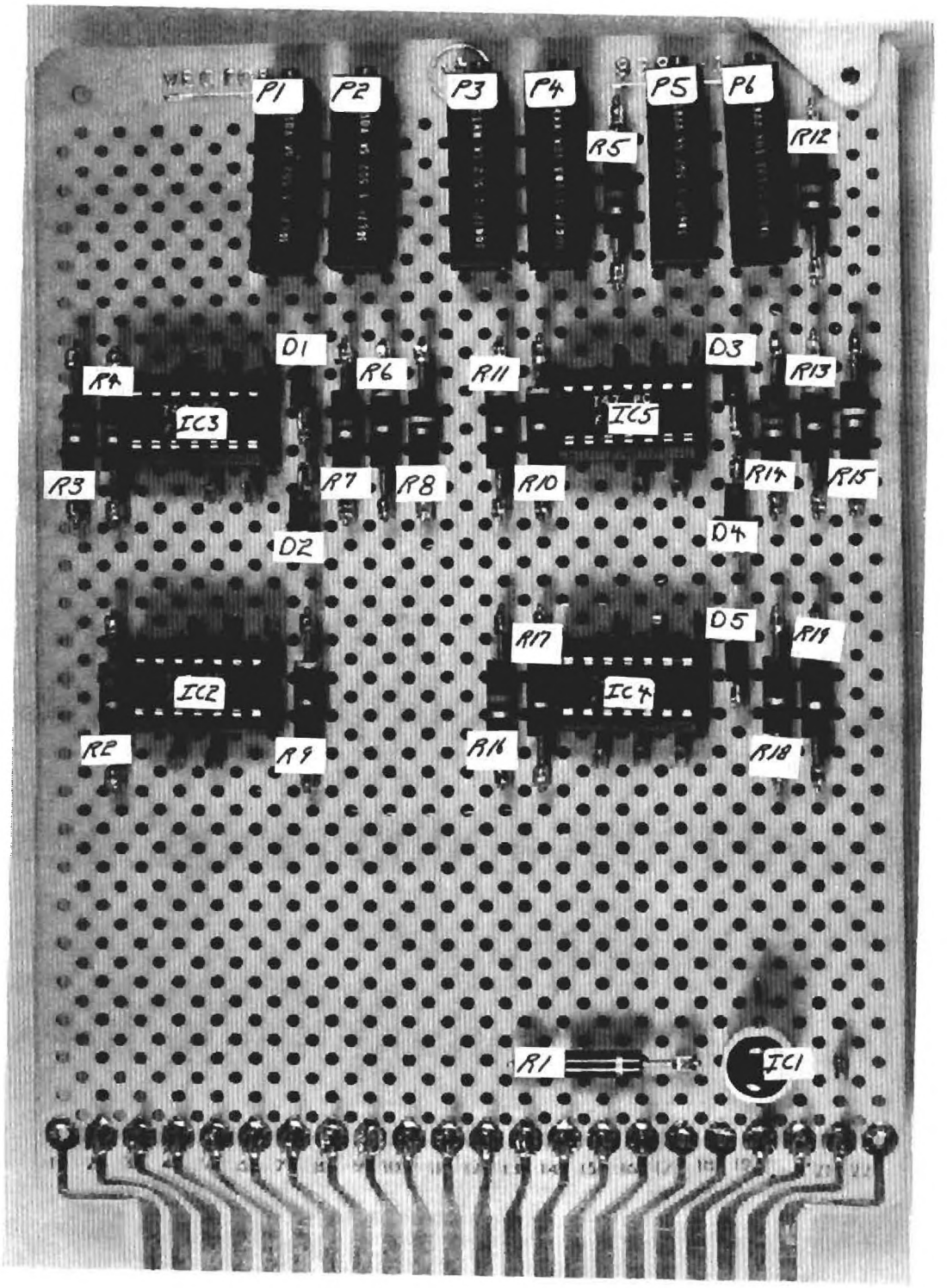


Figure 36. Component Identification Photograph of Board No. 11.

The Azimuth Volts signal enters on T10 and is processed in the same manner as the Elevation Volts signal. The 10 turn, readout azimuth potentiometer on the front panel connects to the board on T2 and T3. The two stages of gain and impedance buffering are built around IC3A and IC3B, with diodes D1 and D2 performing the same function as D3 and D4. The output of IC3B is the Azimuth to Interface signal, is sent out on T14, and is also sent out on T6 through R8 to the front panel azimuth meter.

The Gate Width Select signal enters on T9, is inverted by IC1, and is sent out on T12 to the Interface as the Enable/Disable logic signal.

3.3.2.10 - Backplane Wiring - Figure 37

Pin-to-pin connections between boards are shown in Figure 37.

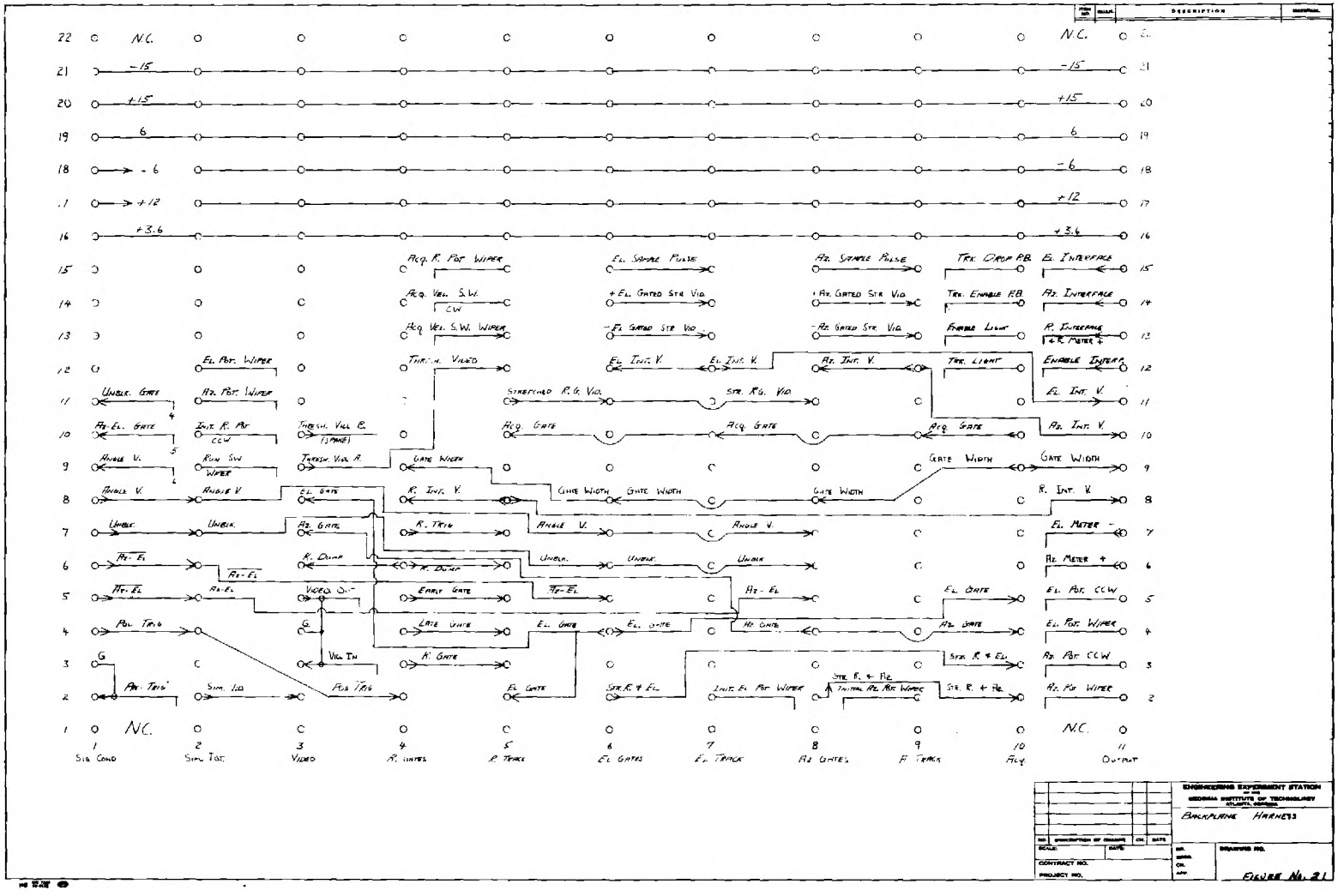


Figure 37. Wiring Diagram of Backplane Harness for Tracking Unit.

SECTION IV

TRACKING UNIT ALIGNMENT PROCEDURES

4.1 Introduction

Test points and trimmer potentiometers have three-digit designations, the first digit corresponding to the plug-in board number and the last digit designating the position on the board. For example, TP203 is located on Board No. 2, and is the third test point from the edge nearest the front panel; P304 is on Board No. 3, and is the fourth trimmer from the front edge. Normally, only the third digits are shown on diagrams of individual boards. TP1 on each board is circuit ground; the ground lead of the test probe may be connected to the chassis or to TP1 on any board, except that for wideband pulses less ringing will be observed in the probe is grounded to TP1 of the board on which the measurement is being made.

Some test points have a series resistor to minimize the circuit loading. Waveforms observed at these points may be slightly degraded, but normally will be adequate to determine whether the circuit is performing properly unless an unusually low-impedance probe is used.

4.2 Board No. 1 - Signal Conditioner - Timing Signals

The two voltages regulated on this board are not critical, and should not require readjustment except when regulator repairs have been made.

4.2.1 +12V Regulator

Connect a DC voltmeter or oscilloscope from TP106 to ground (TP101 or chassis). Turn on main power. Adjust P101 for a reading of +12 volts.

4.2.2 -6V Regulator

Connect a DC voltmeter or oscilloscope from TP107 to ground. Adjust P102 for a reading of -6 volts.

4.3 Board No. 2 - Simulated Target

4.3.1 Video Pulse Width

Temporarily connect a jumper from TP202 to ground, in order to generate a continuous string of simulated video pulses rather than

pulses occurring at particular scan positions. Turn the front panel simulated target function switch to RESET, to hold the pulses at any convenient range determined by the front panel simulated target INITIAL RANGE control. Connect an oscilloscope to TP203 and adjust P201 for a pulse width of 0.2 μs.

4.3.2 Az Sector

Remove the jumper that was placed temporarily from TP202 to ground. Operate the radar in NORMAL mode, with 10-mile range sweep and with the transmitter off. The simulated target should appear on the radar display. Rotate the front panel SIMULATED TARGET AZIMUTH control through its range; the target should move in azimuth on the radar display. Adjust P202 so that the sector covered by the Az control coincides approximately with the display azimuth sector.

4.3.3 El Sector

Rotate the front panel SIMULATED TARGET ELEVATION control through its range; the target should move in elevation on the radar display. Adjust P203 so that the sector covered by the El control coincides approximately with the display elevation sector.

4.3.4 Az Width

Adjust P204 so that the width of the simulated target blip on the radar azimuth display is approximately the same as the blip from an actual aircraft target. As an alternative, the calibrated ARTIFICIAL ANGLE VOLTS potentiometer on the radar display could be used to measure the azimuth extent of the simulated target blip, and P204 adjusted to make the simulated target approximately one beamwidth wide.

4.3.5 El Width

Adjust P205 so that the width of the simulated target blip on the radar elevation indicator is approximately the same as the blip from an actual aircraft target. An alternative method of adjusting P205 is to use the calibrated ARTIFICIAL ANGLE VOLTS potentiometer on the radar display to measure the elevation extent of the simulated target blip, and adjust P205 to make the simulated target approximately one beamwidth wide.

4.4 Board No. 3 - Signal Conditioner - Video

4.4.1 Video Bias

When the tracker is operating, the video input from the receiver-transmitter is summed with the gate markers and simulated target video by means of emitter followers, and the composite video output goes to the radar indicator. Video bias control P301 compensates for the DC level shift in the emitter follower, so that the output video baseline can be adjusted to zero. When the tracker power is turned off, a relay on the video board connects the video input directly to the video output, so the radar can be operated in the normal manner without the tracker.

Connect a DC oscilloscope to TP302 in order to observe the video output. Turn the tracker power on, and operate the radar in the NORMAL mode. Turn P301 clockwise until the baseline on the oscilloscope is observed to rise above ground, then turn P301 counterclockwise just to the point where the baseline stops at zero level. (Note that if P301 is turned further counterclockwise, the video amplitude is reduced by bottom-clipping.)

An alternative method of adjusting video bias is as follows. Connect the oscilloscope to TP302 and stop the radar scan in a position to observe at least one fixed target. Switch the tracker main power alternately on and off, and adjust P301 until the amplitude and DC level of the oscilloscope display with the tracker ON best approximates the display with the tracker OFF.

4.4.2 Threshold A

The composite video signal is compared to a threshold to achieve noise immunity. Connect an oscilloscope to TP303 and observe that the DC voltage varies from zero volts to +3.6 volts as P302 is turned from its totally CCW end to its totally CW end. Set P302 for a threshold voltage of +1.5 volts. This setting has been shown to produce an acceptable trade-off between the probability of detection and the probability of false alarm in previous live tests.

4.4.3 Threshold B

This threshold circuit was included for possible use with gated automatic gain control (GAGC) circuits to be added in the future.

It is not presently used, and may be disabled by leaving P303 in the fully clockwise position.

4.4.4 Marker Amplitude

Adjust P304 for suitable intensity of the gate markers on the display radar. The markers are vertical links on the Az and El displays, showing the location and angular extent of the tracking gates during tracking and of the acquisition window prior to lock-on. They are a few microseconds ahead of the gates in range to avoid obscuring the target blip. Adjustment of gate size is described in a later section.

4.4.5 Simulated Target Amplitude

P305 adjusts the amplitude of the simulated target video pulse. If it is set below the threshold level, it may be visible on the display but cannot be tracked. Temporarily place a jumper from TP202 to ground to make the simulated target appear at all angles for easy identification. Connect an oscilloscope to TP302. Set the simulated target function switch on the front panel to RESET and set the simulated target initial range control on the panel to a convenient range for viewing on the scope. Adjust P305 so that the simulated target pulse is the same amplitude as saturated targets. Remove the jumper from TP202.

4.5 Board No. 4 - Range Gates

4.5.1 Wide Gate Start

Connect an oscilloscope to TP402 to view the negative-going early gate. Press the front panel TRACK DROP push button, to ensure that the gates are in their wide state. Adjust P401 for the desired width of the early gate. Initial adjustment was made for a half-gate width of 1 μsec (2 μsec full width of the acquisition range gate); the adjustment can be changed to other widths as experience dictates.

4.5.2 Wide Gate End

Connect the scope to TP403 to view the negative-going late gate. Adjust P402 for a late gate width as nearly possible identical to the early gate as adjusted above. If the scope has the capability of displaying two separate vertical inputs on alternate traces, it is convenient

to connect one probe to TP402 and the other to TP403, trigger the scope internally to superimpose the early and late gates on the scope, and adjust P401 and P402 for early and late gates of the desired widths. Identical width of the early and late gate is more important that the particular width chosen.

4.5.3 Narrow Gate Start

Connect the scope to TP402, press the TRACK DROP push button, and connect on jumper from TP1005 (Board No. 10) to ground in order to switch to the narrow gates used in tracking. Adjust P403 for the desired width of the narrow early gate. Initial adjustment was made for a width of 0.2 μsec.

4.5.4 Narrow Gate End

Connect the scope to TP403, with the jumper remaining from TP1005 to ground. Adjust P404 for a narrow late gate width with the same as the early gate. As described in 4.5.2 above, it is convenient to connect the two probes of an alternate-trace scope to TP403 and TP404, and adjust P403 and P404 until the early and late gates coincide. Remove the jumper from TP1005 after the adjustment is completed, unless it is intended to proceed directly to the next step below.

4.6 Board No. 5 - Range Track

4.6.1 Gate Balance

The width of the early and late gates must be made equal as described in 4.5.2 and 4.5.4 above, prior to making this adjustment. Connect a DC voltmeter from TP504 to ground. Press the TRACK DROP push button. Connect a jumper from TP502 to TP503 to simulate the presence of a video signal for the entire gate width. Connect a jumper from TP1005 (Board No. 10) to ground to switch to the narrow gate width. Adjust P501 for zero reading of the voltmeter of TP504. Remove the jumper from TP1005 to return to the wide pulse; the voltmeter should continue to read near zero. If the reading on wide pulse is outside ± 0.5 volt after adjustment to zero on narrow pulse, recheck adjustments in 4.5.2 and 4.5.4.

4.6.2 Range Tracking Loop Gains

The two significant parameters in the range tracking loop are the integrator gain KR_2 and the proportional gain KR_3. These gains are adjusted by means of potentiometers P502 and P503, respectively. The integrator gain KR_2 is equal to 0.23 when potentiometer P502 is positioned fully CW, and decreases to zero as P502 is turned fully CCW. The proportional gain KR_3 is equal to 0.50 when potentiometer P503 is positioned fully CW, and decreases to zero as P503 is turned fully CCW. Recommended values for KR_2 and KR_3, respectively, as obtained from simulation, are 0.12 and 0.25. These values for the gains are obtained by positioning potentiometer P502 ten turns CW from the fully CCW position and potentiometer P503 ten turns CW from the fully CCW position.

4.7 Board No. 6 - Elevation Gates

4.7.1 Wide Gate Width

The two halves of the split elevation gate are designated the - Gate and the + Gate. The - Gate is the lower half-gate, and the + Gate is the upper half-gate.

Set an oscilloscope for external sweep and connect its external horizontal input to TP105 (Board No. 1), in order to sweep the scope with Angle Volts. Connect the scope probe to TP104 (Board No. 1) so that the Az-El unblanking pulses provide vertical deflection. Operate the radar in NORMAL mode, with the transmitter off. Note that the oscilloscope horizontal trace follows the normal scan sequence of Az followed by El in one direction, then Az followed by El in the other direction. The elevation scans are the shorter traces. Adjust the scope sweep length and position so that the elevation scans extend between the outermost vertical lines of the graticule with the positive blanking pulses just outside the graticule lines; the azimuth scans will extend beyond the right-hand edge of the scope face.

Move the scope probe from TP104 to TP602, in order to view the elevation - Gate. Press the TRACK DROP push button to ensure that the gates are in their wide state and positionable by means of the front-panel

controls. Adjust the ACQUISITION ELEVATION control so that the right-hand edge of the - Gate (corresponding to the center of the full gate) coincides with the center vertical line of the graticule. Adjust P601 for the desired width of the elevation half-gate. Initial adjustment was made for a width of 2 cm on the 10 cm graticule. Since the 10 cm trace corresponds approximately to the 11° elevation scan, this half-gate width is approximately 2.2", corresponding to a full gate of approximately 4.4°. This wide gate is the elevation extent of the acquisition window. Its position is shown by a marker on the radar's elevation display, at a range set by the ACQUISITION RANGE control.

4.7.2 Narrow Gate Width

Leave all connections as in 4.7.1 above, and place a jumper from TP1005 (Board No. 10) to ground in order to switch to the narrow gate. Adjust P602 for the desired elevation half-gate width. Initial adjustment was made for a width of 0.4 cm on the 10 cm scope trace, corresponding approximately to 1.2° half-gate width, or 2.4° full gate. This narrow gate is the elevation tracking gate.

4.7.3 Width Balance

Note carefully the width of the narrow - Gate in 4.7.2 above, and if possible position it so that its two ends coincide with vertical marks on the graticule. Move the scope probe from TP602 to TP603 in order to view the + Gate. Its left-hand edge will coincide with the right-hand edge of the - Gate. Adjust P603 so that the + Gate is the same width as the - Gate. Equality of the + and - gate widths is more important than the particular width chosen.

Remove the jumper from TP1005 to return to wide gates. Note the width of the - Gate, then move the probe from TP603 back to TP602 to view the + Gate. The two wide half-gates should be very nearly equal. The same adjustment, P603, balances the widths of both wide and narrow elevation gates. If there is any discrepancy, the adjustment should be made for equal narrow gates in the interest of tracking accuracy.

4.8 Board No. 7 - Elevation Track

4.8.1 Gate Balance

The width of the + and - elevation gates must be equalized as

described in 4.7.3 above, prior to making this adjustment. Connect the input of a DC oscilloscope from TP703 to ground. Connect a jumper from TP505 (Board No. 5) to ground in order to simulate the presence of a target throughout the elevation gate. Connect another jumper from TP1005 (Board No. 10) to ground in order to switch to narrow gates. Press the TRACK DROP push button. Position the gate marker on the radar display near the center of the elevation scan by means of the ACQUISITION ELEVATION control. Note that the vertical position of the scope trace (voltage on TP703) may wander slightly from scan to scan. Adjust P701 so that the mean DC level of the scope track is zero volts. It should wander less than ± 0.5 volt. Remove the jumpers from TP1005 and TP505.

4.8.2 Maximum Initial Elevation

Operate the radar in NORMAL mode with the transmitter off. Press the TRACK DROP push button. Rotate the front-panel ACQUISITION ELEVATION control through its range; the elevation gate marker on the radar display should move in elevation. Adjust P702 so that the center of the gate marker is approximately at the top of the elevation scan when the ACQUISITION ELEVATION control is fully clockwise.

4.8.3 Elevation Tracking Loop Gains

The two significant parameters in the elevation tracking loop are the integrator gain KE_2 and the proportional gain KE_3. These gains are adjusted by means of potentiometers P703 and P704, respectively. The integrator gain KE_2 is equal to .1 when potentiometer P703 is positioned fully CW and decreases to zero as P703 is turned fully CCW. The proportional gain KE_3 is equal to 1 when potentiometer P704 is positioned fully CW, and decreases to zero as P704 is turned fully CCW. Recommended values for KE_2 and KE_3. respectively, as obtained from simulation, are .04 and .4. These values for the gains are obtained by positioning potentiometer P703 eight turns CW from the fully CCW position and potentiometer P704 eight turns CW from the fully CCW position.

4.9 Board No. 8 - Azimuth Gates

4.9.1 Wide Gate Width

Refer to 4.7.1. Alignment of the azimuth gates is analogous to the alignment of the elevation gates. The Azimuth - Gate is the early

gate during counterclockwise azimuth scans and the late gate during clockwise scans; the Azimuth + Gate is the early gate during clockwise scans and the late gate during counterclockwise scans.

Connect the oscilloscope for external sweep as in 4.7.1, with the horizontal input on TP105 and the probe on TP104. Readjust the scope sweep length and position, so that the azimuth scan (the longer of the alternate traces) just fills the width of the scope graticule, with positive blanking pulses just outside the graticule lines. Ignore a blanking pulse that occurs near the center of the trace, corresponding to the beginning of a downward elevation scan.

Move the scope probe from TP104 to TP802, in order to view the azimuth - Gate. Press the TRACK DROP push button to ensure that the gates are in their wide state and positionable by means of the front-panel controls. Adjust the ACQUISITION AZIMUTH control so that the right-hand end of the - Gate (corresponding to the center of the full gate) coincides with the vertical center line of the graticule. Adjust P801 for the desired width of the azimuth half-gate. Initial adjustment was made for a width of 2 cm on the 10 cm graticule. Since the 10 cm trace corresponds approximately to the 30° azimuth scan, this half-gate width is approximately 6°, corresponding to a full gate of approximately 12°. This wide gate is the azimuth extent of the acquisition window. Its position is shown by a marker on the radar's azimuth display, at a range set by the ACQUISITION RANGE control.

4.9.2 Narrow Gate Width

Leave all connections as in 4.9.1 above, and place a jumper from TP1005 (Board No. 10) to ground in order to switch to the narrow gate. Adjust P802 for the desired azimuth half-gate width. Initial adjustment was made for a width of 0.4 cm on the 10 cm scope trace, corresponding approximately to 1.2° half-gate width, or 2.4° full gate. This narrow gate is the azimuth tracking gate.

4.9.3 Width Balance

After the narrow - Gate is adjusted to the desired width as in 4.9.2, readjust the scope external sweep gain and position so that the

two ends of the - Gate coincide with two vertical lines near the center of the scope graticule. Move the scope probe from TP802 to TP803 in order to view + Gate. Its left-hand edge will coincide with the right-hand edge of the - Gate. Adjust P803 so that the + Gate is the same width as the - Gate. Equality of the + and - gate widths is more important than the particular width chosen.

4.10 Board No. 9 - Azimuth Track

4.10.1 Gate Balance

The width of the + and - azimuth gates must be equalized as described in 4.9.3 above, prior to making this adjustment. Connect the input of a DC oscilloscope from TP903 to ground. Connect a jumper from TP505 (Board No. 5) to ground to simulate the presence of a target throughout the azimuth gate. Connect another jumper from TP1005 (Board 10) to ground in order to switch to narrow gates. Press the TRACK DROP push button. Position the gate marker on the radar display near the center of the azimuth scan by means of the ACQUISITION AZIMUTH control. Note that the vertical position of the scope trace (voltage on TP903) may wander slightly from scan to scan. Adjust P901 so that the mean DC level of the scope trace is zero volts. It should wander less than ± 0.5 volt. Remove the jumpers from TP1005 and TP505.

4.10.2 Maximum Initial Azimuth

Operate the radar in NORMAL mode with the transmitter off. Press the TRACK DROP push button. Rotate the front-panel ACQUISITION AZIMUTH control through its range; the azimuth gate marker on the radar display should move in azimuth. Adjust P902 so that the center of the gate marker is approximately at the top of the azimuth scan when the ACQUISITION AZIMUTH control is fully clockwise.

4.10.3 Azimuth Rate Gain and Azimuth Gain

The two significant parameters in the azimuth tracking loop are the integrator gain KA_2 and the proportional gain KA_3. These gains are adjusted by means of potentiometers P903 and P904, respectively. The integrator gain KA_2 is equal to .1 when potentiometer P903 is positioned fully CW, and decreases to zero as P903 is turned fully CCW. The proportional

gain KA_3 is equal to 1 when potentiometer P904 is positioned fully CW, an decreases to zero as P904 is turned fully CCW. Recommended values for KA_2 and KA_3 respectively, as obtained from simulation, are .06 and .6. These values for the gains are obtained by positioning potentiometer P903 4.75 turns CW from the fully CCW position and potentiometer P904 twelve turns CW from the fully CCW position.

4.11 Board No. 10 - Acquisition

4.11.1 Hits to Acquire

After the TRACK ENABLE push button is pressed, either one of the following two conditions causes the gates to sense the presence of a target and attempt to acquire it: (1) a preset number of video pulses above the video threshold within the wide range gate and within the wide elevation gate during any elevation scan, followed by a preset number of video pulses above the threshold within the wide range gate and within the wide azimuth gate during the next azimuth scan, or (2) a preset number of video pulses above the threshold within the wide range gate and within the wide azimuth gate on any azimuth scan, followed by a present number of video pulses above the threshold within the wide range gate and within the wide elevation gate during the next elevation scan. These conditions are met if a target within the acquisition window in range, elevation, and azimuth produces the preset number of pulses above the threshold on each of two successive scans.

The preset number of pulses required for acquisition is adjusted by means of P1001 as an analog time delay. Initial adjustment was made at approximately 5 hits per scan to acquire, by the following procedure.

Connect an oscilloscope to TP1002. Place a jumper from TP505 (Board No. 5) to ground to simulate the presence of a target for the entire gate duration. Note that the scope trace is at a positive voltage throughout most of each scan, with a short negative-going ramp followed by a positive-going ramp each time the azimuth gate occurs. Trigger the scope with the negative-going edge of the azimuth gate at TP804 (Board No. 8) and adjust the sweep length so that the negative-going ramp at TP1002 occupies a major portion of the scope trace. Adjust P1001 so that the negative ramp crosses

zero volts approximately 4 milliseconds after its beginning. (This time delay is approximately 5 interpulse periods of the radar, for acquisition on 5 hits per scan. Adjustment may be made for a different delay as experience dictates.) The time delay in elevation will be approximately the same as in azimuth. It may be verified, if desired, by moving the scope probe from TP1002 to TP1003 and moving the external trigger cable from TP804 to TP604. After adjustment is completed, remove the jumper from TP505.

4.11.2 Narrow Gate Delay

The range, elevation, and azimuth gates remain wide for a preset time after acquisition to permit stabilization of the tracking loops, then switch to their narrow width for the remainder of the tracking time. Two panel lights indicate the gate condition, as follows. The amber ENABLE light comes on when the ENABLE push button is pressed. The green TRACK light comes on when a target is acquired, and both lights remain on until the gates switch to narrow or the target is dropped. The amber light is extinguished, leaving only the green light on, when the gates switch to narrow; the gate markers on the radar display become narrow at that time. Both lights are extinguished when the target is dropped; the gate markers on the radar indicator widen and return to the present acquisition window position when the target is dropped. After a target is dropped, the ENABLE push button must be pressed again before the same or another target can be acquired.

The time delay between acquisition and gate narrowing is adjusted by means of P1002. Operate the radar in NORMAL mode with the transmitter off. Press the ENABLE push button, and note that the amber ENABLE light is on. Place a jumper from TP505 (Board No. 5) to ground; observe that the green light comes on immediately and the amber light is extinguished after a time delay. Estimate this time delay by counting seconds mentally, by counting radar scans, or by using the second hand of a watch. Initial adjustment was made for approximately 8 seconds delay (8 azimuth scans and 8 elevation scans). If the observed delay is not the desired time, turn P1002 clockwise to increase delay or counterclockwise to decrease delay. Remove the ground from TP505, wait for the lights

to extinguish, press the ENABLE push button, ground TP505, and observe the new time delay. Repeat the above procedure until a suitable delay is achieved.

4.11.3 Drop Delay

Any time after acquisition, if the target is missed in range or elevation or azimuth for a preset time, the track is dropped. The delay time between a missed target and track drop is adjusted by means of P1003. Depending on the purpose for which the tracker is used, it may be desirable to drop track immediately when the target is missed on a single scan to avoid the possibility of sending false information to the aircraft, or it may be desirable to let the gates "coast" for several seconds in hope of reacquiring automatically. Note that there is little that the operator can do to assist in this reacquisition, because the gate position controls are disabled in the tracking mode. If the target range is sufficient, the operator can attempt to reacquire after track drop by moving the acquisition window to a position ahead of the approaching target and pressing the ENABLE push button. He can drop track at any time, without waiting for the time delay, by pressing the DROP push button.

During the initial adjustment of the tracking loops, before successful tracking is attained, P1003 may be turned fully clockwise for maximum drop delay so that the operator will have time to observe which tracking gate is first to drift off the simulated target in repeated attempts to acquire. Each attempt can be terminated at the desired time by pressing the DROP push button and turning the simulated target switch to RESET.

After adjustment of the tracking loops so that successful tracking of the simulated target is possible, adjust P1003 to drop track after the desired number of missed scans as follows. Set the simulated target to fly in at angles near the center of the azimuth and elevation scans, acquire the simulated target, and allow sufficient time for the gates to narrow and for tracking to stabilize. Watch the radar display. When the target blip completes a paint on one of the scans, turn the simulated target switch to RESET. Note the number of additional scans that occur before the gates widen and begin to return to their acquisition

position. If this observed drop delay is not the desired value, turn P1003 clockwise to increase the delay or counterclockwise to decrease the delay. Note that the earliest practical drop time is at the end of the paint of the gate markers on the next scan, since that will be the first scan for which the target is absent.

4.12 Board No. 11 - Output

4.12.1 Range Zero

Set the Simulated Target Function switch to RESET. Move the simulated target blip to zero range (coincident with the touchdown marker on the radar indicator) by means of the Simulated Target INITIAL RANGE control. Press the TRACK ENABLE push button, and move the acquisition gates to acquire the simulated target in its zero-range position. Adjust P1101 so that the RANGE meter reads zero.

4.12.2 Range Gain

Move the simulated target blip until it coincides with the 8-mile marker on the radar indicator, by means of the simulated target INITIAL RANGE control. Press the TRACK ENABLE push button, and move the acquisition gates to acquire the simulated target in its 8-mile position. Adjust P1102 so that the RANGE meter reads 8 (nmi).

Repeat steps 4.11.1 and 4.11.2 as required, to compensate for any interaction between P1101 and P1102, noting that P1101 calibrates the RANGE meter at zero range, and P1102 calibrates the RANGE meter at any desired point near maximum range. Move the simulated target to its maximum range, set the Simulated Target Function switch to RUN, and acquire the target as it flies inward. Note the reading of the RANGE meter each time the simulated target crosses a range marker on the radar indicator.

4.12.3 Azimuth Potentiometer Calibration

The multi-turn azimuth potentiometer to the right of the AZIMUTH meter sets the courseline reference. No provision is made in the present circuit to compensate for offset of the radar from runway centerline; therefore, the AZIMUTH potentiometer selects a constant azimuth angle from radar to target for which the AZIMUTH meter reads zero. The AZIMUTH potentiometer is calibrated by means of P1103. The intended calibration coincides

with the ARTIFICIAL ANGLE VOLTS potentiometer on the radar indicator, and is 10 counts per degree. Zero reading of the potentiometer dial corresponds to 15 degrees clockwise from scan center; 150 counts on the dial corresponds to scan center; 300 counts on the dial corresponds to 15 degrees counterclockwise from scan center.

Assume that the ARTIFICIAL ANGLE VOLTS potentiometer on the radar indicator has been calibrated properly. Set it to 250 counts, move the ANGLE VOLTS switch above it momentarily to AZ and back to center. A horizontal line with some persistance will be painted on the azimuth indicator at +10 degrees (25 degrees from the lower edge of the azimuth scan). Place the Simulated Target Function switch on RESET, and position the simulated target blip in azimuth so that it is bisected by this +10 degree line. Press the TRACK ENABLE push button and move the acquisition gates to acquire the simulated target in this stationary position. Set the AZIMUTH potentiometer on the tracker panel to 250 counts. Adjust P1103 so that the AZIMUTH meter reads zero. The AZIMUTH potentiometer has now been calibrated to coincide with the radar's ARTIFICIAL ANGLE VOLTS potentiometer as a setting of 250 counts, it is expected to track reasonably well over the remainder of its range because of the linearity of the potentiometers.

4.12.4 Azimuth Gain

Sensitivity of the AZIMUTH meter is calibrated to ± 2.5 degrees full scale by means of P1104. After completing step 4.11.3, with the tracking gates still locked on the stationary simulated target, turn the AZIMUTH potentiometer to 275 counts (25 counts, or 2.5 degrees, from the previous setting). Adjust P1104 so that the AZIMUTH meter reads full-scale. The meter sensitivity is now calibrated for 2.5 degrees full scale. Turn the AZIMUTH potentiometer to 225 counts. The meter should read full scale in the opposite direction.

4.12.5 Elevation Potentiometer Calibration

The multi-turn ELEVATION potentiometer to the right of the ELEVATION meter selects the glidepath reference angle. No provision is made in the present circuit to compensate for distance from the radar to touchdown, therefore, the ELEVATION potentiometer selects a constant elevation angle from radar to target for which the ELEVATION meter reads

zero. The ELEVATION potentiometer is calibrated by means of P1105. The intended calibration coincides with the ARTIFICIAL ANGLE VOLTS potentiometer on the intended radar indicator, and is 20 counts per degree. Zero reading of the potentiometer dial corresponds to -1 degree, and 220 counts on the dial corresponds to +10 degrees.

Assume that the ARTIFICIAL ANGLE VOLTS potentiometer on the radar indicator has been calibrated properly. Set it to 180 counts, move the ANGLE VOLTS switch above it momentarily to EL and back to center. A horizontal line with some persistence will be painted on the elevation indicator at +8 degrees (9 degrees above the lower edge of the elevation scan). Place the Simulated Target Function switch on RESET, and position the simulated target blip in elevation so that it is bisected by this +8 degree line. Press the TRACK ENABLE push button and move the acquisition gates to acquire the simulated target in this stationary position. Set the ELEVATION potentiometer on the tracker panel to 180 counts. Adjust P1105 so that the ELEVATION meter reads zero. The ELEVATION potentiometer has now been calibrated to coincide with the radar's ARTIFICIAL ANGLE VOLTS potentiometer at a setting of 180 counts; it is expected to track reasonably well over the remainder of its range because of the linearity of the potentiometers.

4.12.6 Elevation Gain

Sensitivity of the ELEVATION meter is calibrated to ± 0.7 degree full scale by means of P1106. After completing step 4.11.5, with the tracking gates still locked on the stationary simulated target, turn the ELEVATION potentiometer to 194 counts (14 counts, or 0.7 degree, from the previous setting). Adjust P1106 so that the ELEVATION meter reads full scale. The meter sensitivity is now calibrated for 0.7 degree full scale. Turn the ELEVATION potentiometer to 166 counts. The meter should read full scale in the opposite direction.

SECTION V
INTERFACE UNIT TECHNICAL DESCRIPTION

5.1 Introduction

The purpose of the Interface Unit is the conversion of aircraft position data obtained from the AN/TPN-8 tracker into two forms: a Pseudo ILS modulation signal and a binary signal compatible with the Research Communications Industries Special Data Link (SDL)[1]. As described earlier in Section II, the Pseudo ILS signal conveys a measure of vertical and lateral displacement of the aircraft from the desired approach path; the SDL signal conveys the vertical and lateral displacement data as well as range-to-touchdown information.

The Interface Unit consists of two sections which are called the ILS section and the SDL section. The ILS section converts the tracker output glideslope and courseline deviation voltages into Pseudo ILS signals for input into an ILS transmitter. The ILS section contains two physically identical channels: one for the azimuth, or courseline data and the other for the elevation, or glideslope data. Respective inputs are scaled in each channel and used to simultaneously modulate two audio frequency (90 Hz and 150 Hz) tones which are added and transmitted to the aircraft via an ILS transmitter. The SDL section accepts range data as well as glideslope and courseline data, and formats the data into a fourteen bit binary word compatible with the SDL. The SDL section contains three channels, one each for range, azimuth, and elevation data. Each channel scales its input signal and feeds it to the analog switch for time-shared transmission. The "data selector" gates the analog switches such that each channel is interrogated in succession; it also generates a two bit channel code for identification of the data. The output of the selected channel is converted to binary form by an eight bit A/D converter. The output word to the SDL transmitter is composed of this eight bit number, the function (channel) identification code, a data-ready pulse, and an aircraft identification code.

5.2 Functional Description

The Interface Unit block diagram in Figure 38 shows that the ILS section and the SDL section are functionally independent. Accordingly, they are described separately in the following.

5.2.1 ILS Section

The two audio tone frequencies used in the ILS Interface, 90 and 150 Hz, are derived from a crystal controlled 90 KHz oscillator, Figure 39. The 90 KHz signal is applied to two frequency division chains which divide by 600 and by 1000 to produce 150 Hz and 90 Hz square waves, Figures 40 and 41. The square waves are converted to sinusoidal waves by 2 sets of active four-pole, R-C lowpass filters, Figures 42 and 43. The two tones are then amplified to a level of 10 volts (peak-to-peak) and applied to the azimuth and elevation channel modulators, Figures 44, 45, 46 and 47.

The angular deviation signals from the AN/TPN-8 tracker enter via J1 and are processed by the scalers which amplify and add a constant to each (azimuth, elevation) deviation signal. In this way, the behavior of the input can be modified to obey any linear equation for accounting for angular offsets. The inverting scaler output forms the modulating voltage for the 150 Hz tone, and the noninverting scaler output is the modulating voltage for the 90 Hz tone. Figures 48 and 49 show graphs of the relative behavior of the modulated 150 and 90 Hz tones for the azimuth and elevation channels, respectively. The two tones are mixed together and transmitted to the aircraft via the proper (glideslope or courseline) ILS transmitter.

5.2.2 SDL Section

In the SDL section of the Interface Unit, the range, azimuth, and elevation voltages from the AN/TPN-8 tracker are processed by separate noninverting scalers located on Board No. 5, Figures 50 and 51, similar to those in the ILS section. The azimuth and elevation scalers are identical. The range scaler, however, contains a log amplifier which makes its output proportional to the log of target range. Angular deviation and range voltages from the tracker are adapted to the analog-to-digital converter by the three scalers. Each scaler output is connected to an analog switch which is exclusively turned on by a request from the Data Selector/Digitizer, located on Board No. 6, Figures 52 and 53.

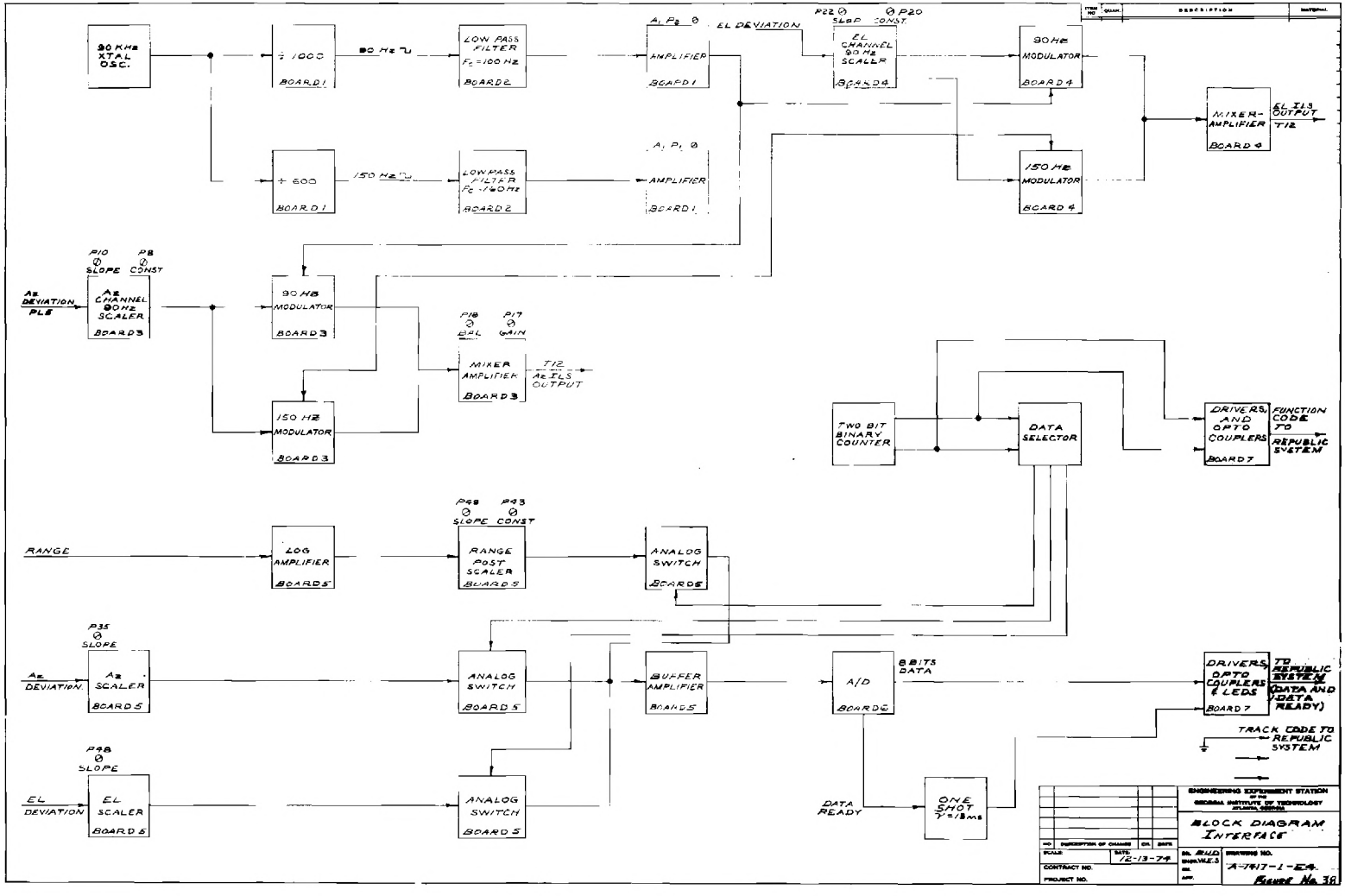


Figure 38. Interface Block Diagram

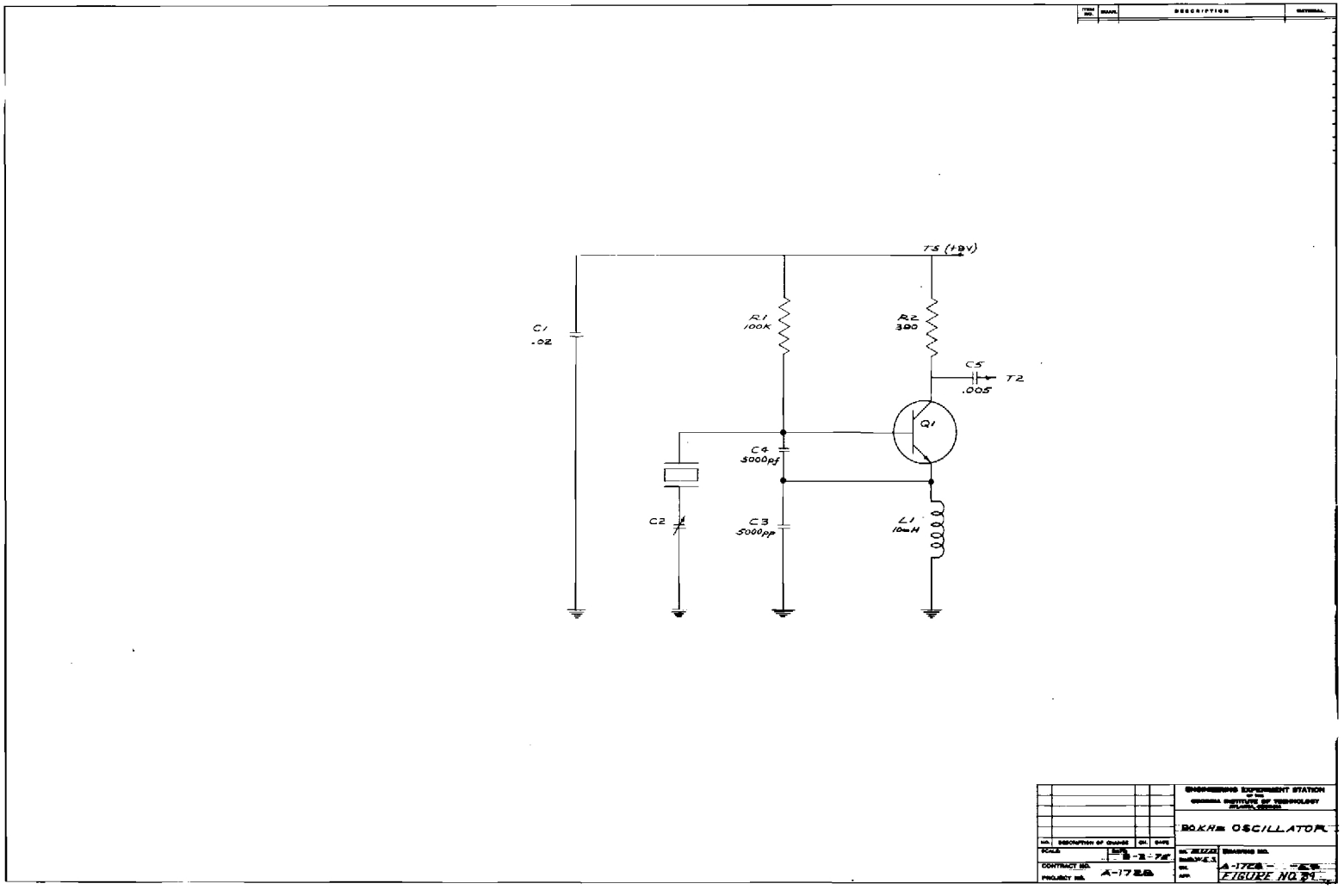


Figure 39. Basic 90 KHz Oscillator.

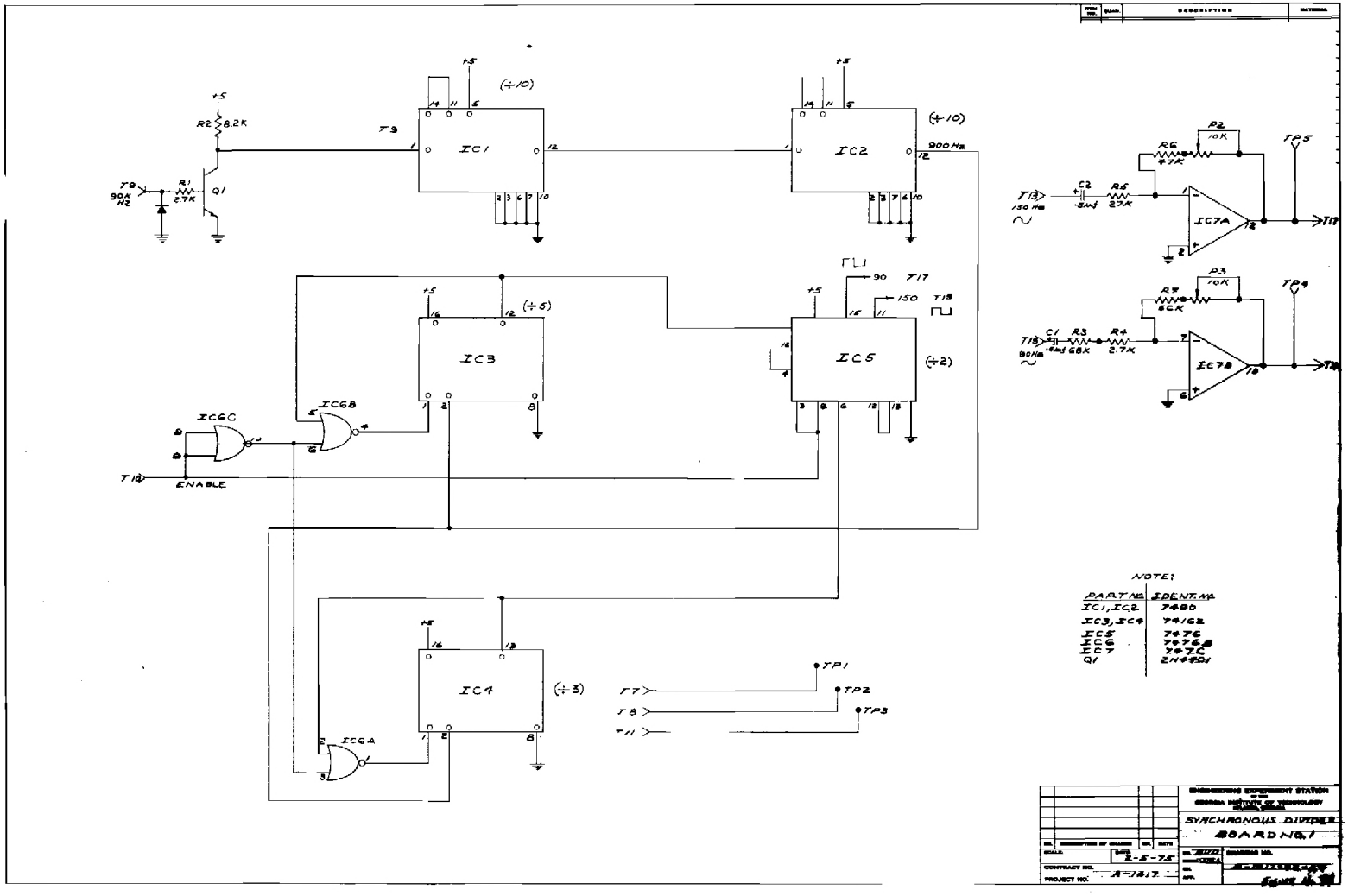


Figure 40. Schematic Diagram of Board No. 1.

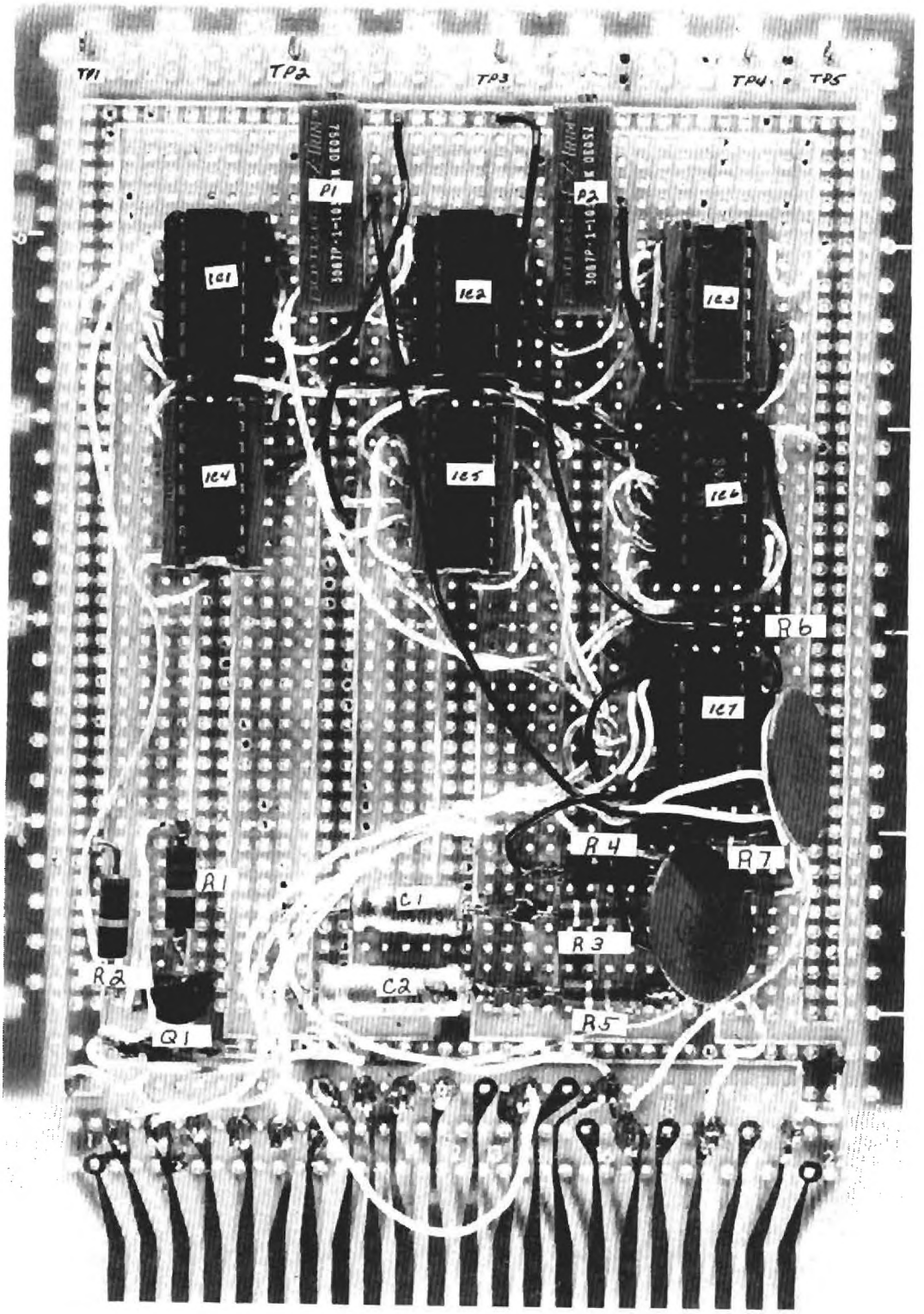


Figure 41. Component Identification Photograph of Board No. 1.

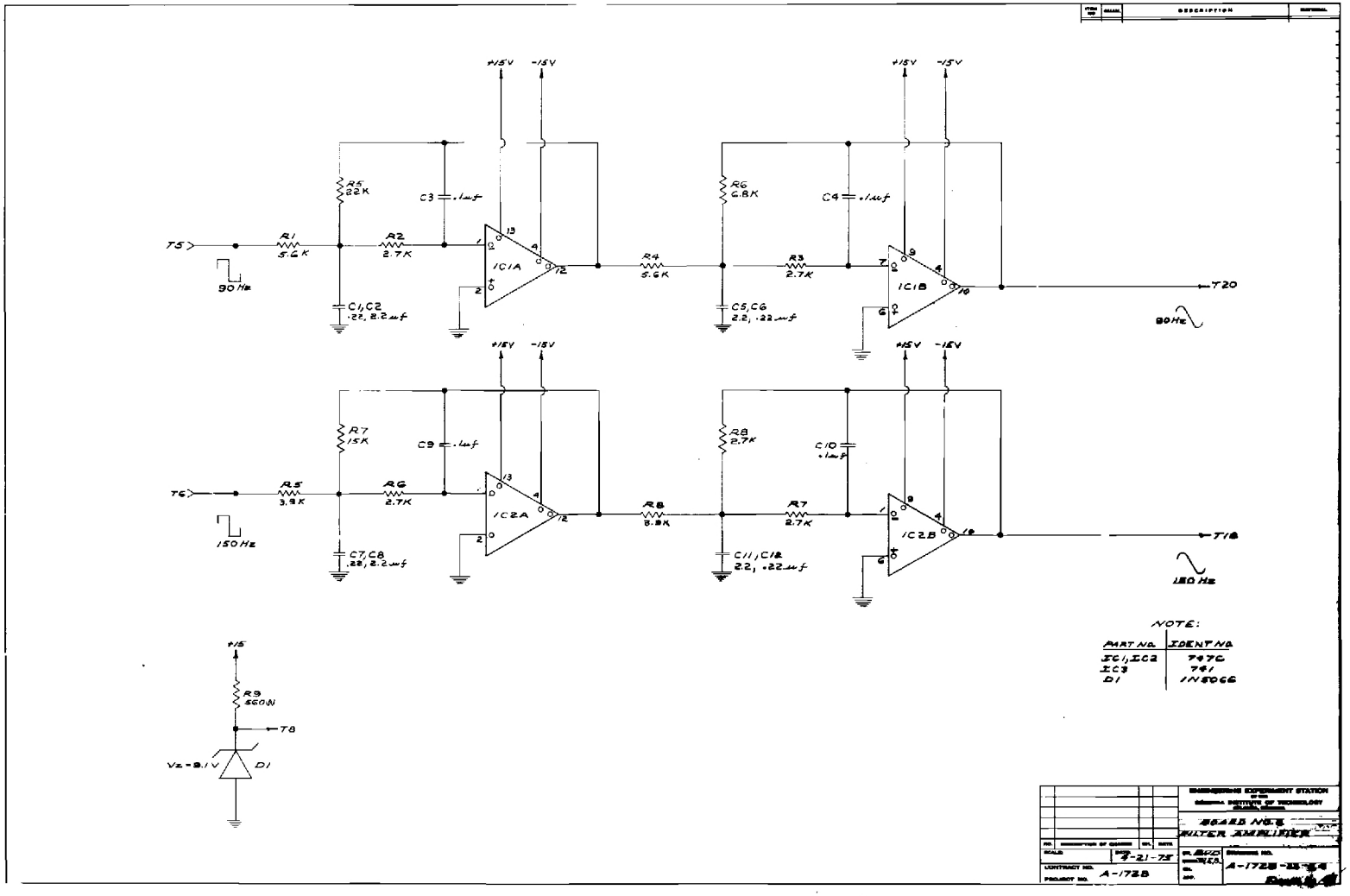


Figure 42. Schematic Diagram of Board No. 2.

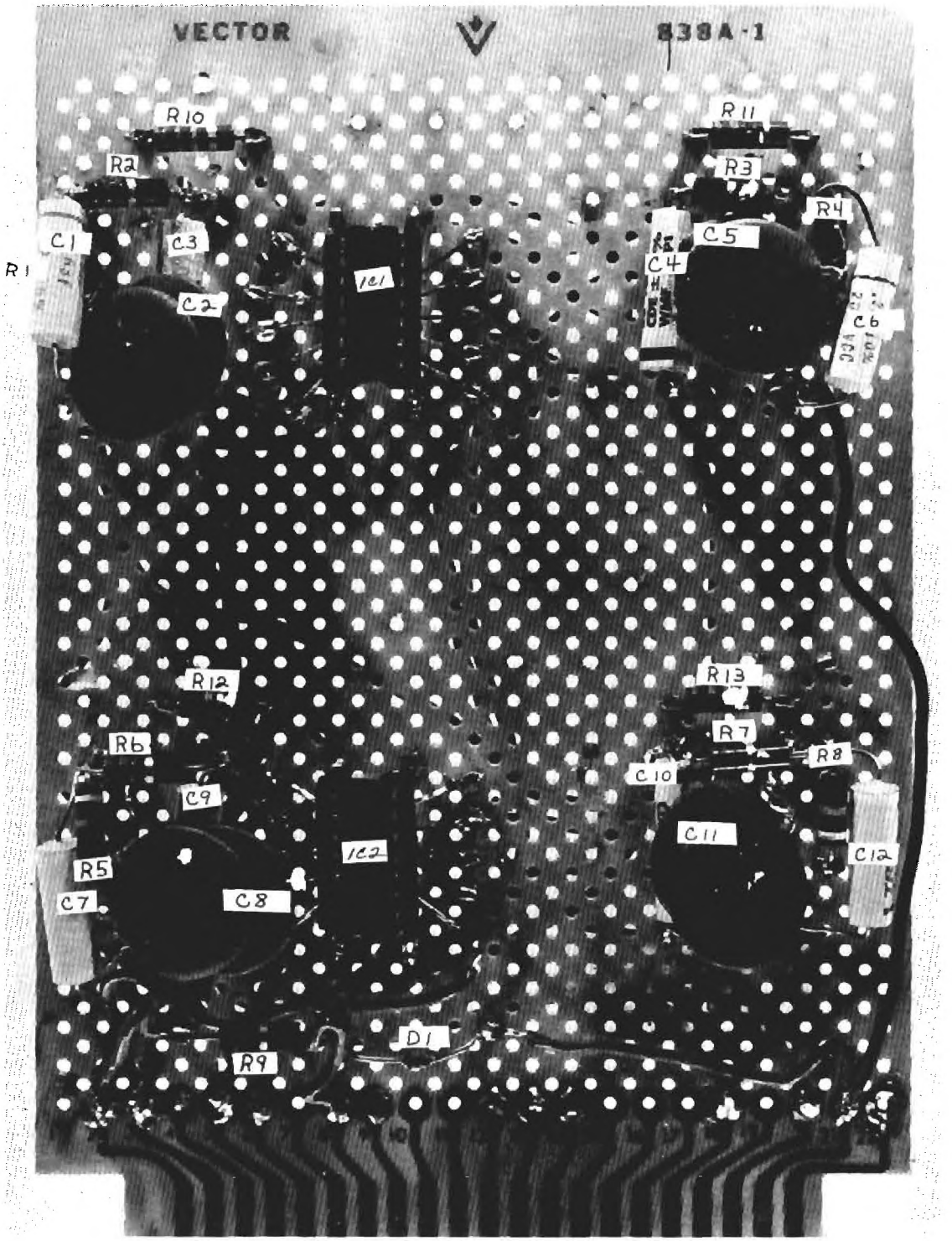


Figure 43. Component Identification Photograph of Board No. 2.

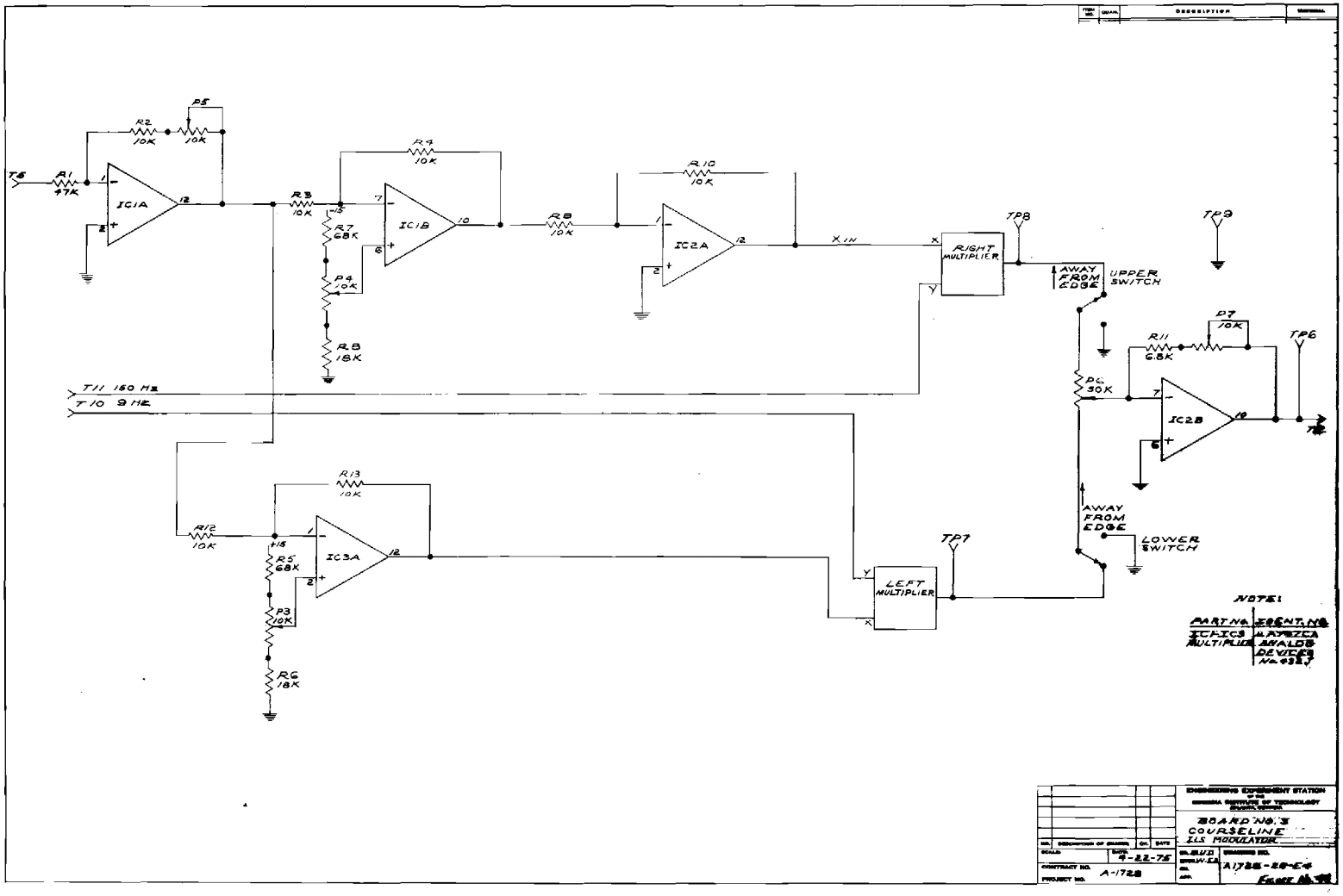


Figure 44. Schematic Diagram of Board No. 3.

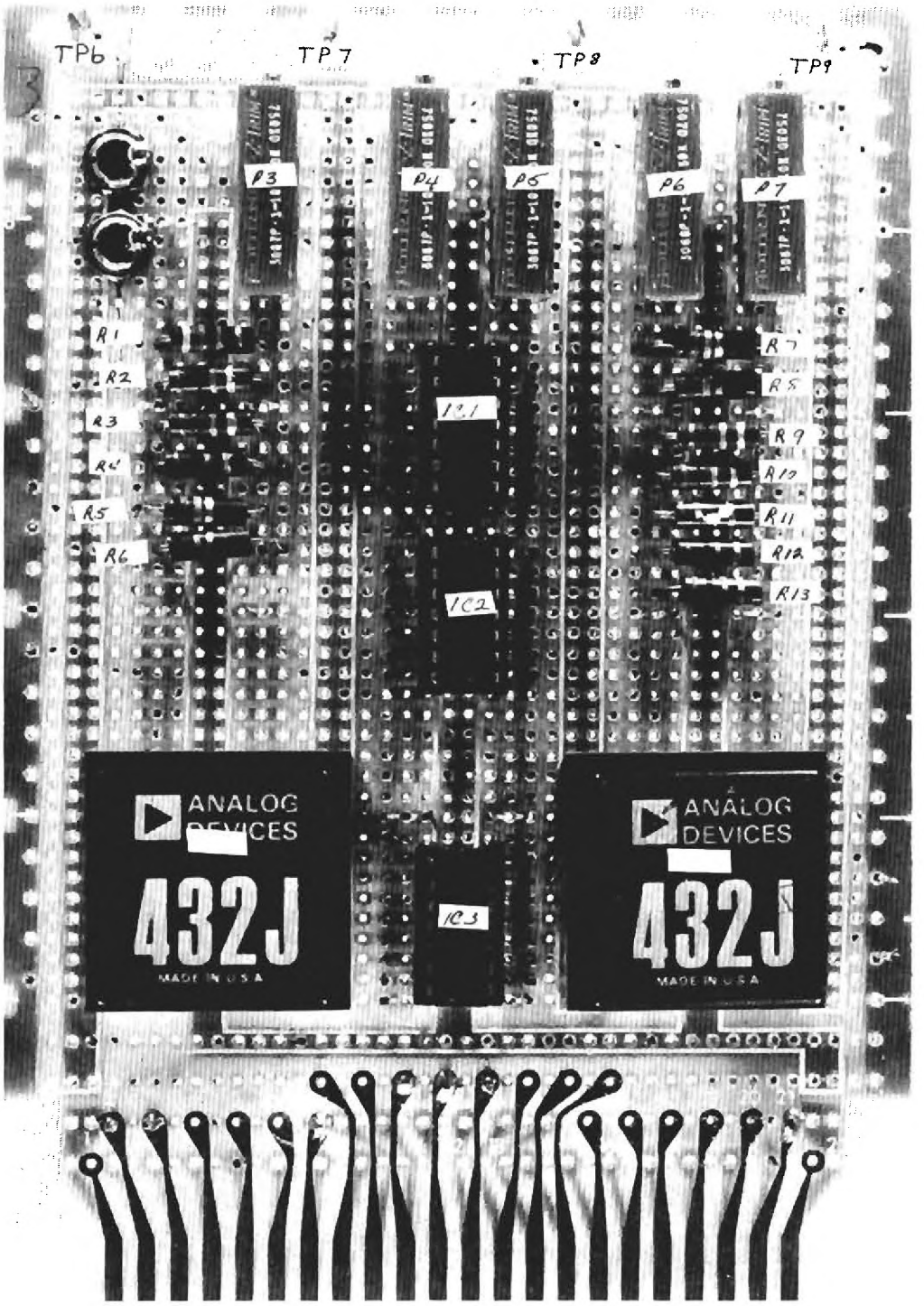


Figure 45. Component Identification Photograph of Board No. 3.

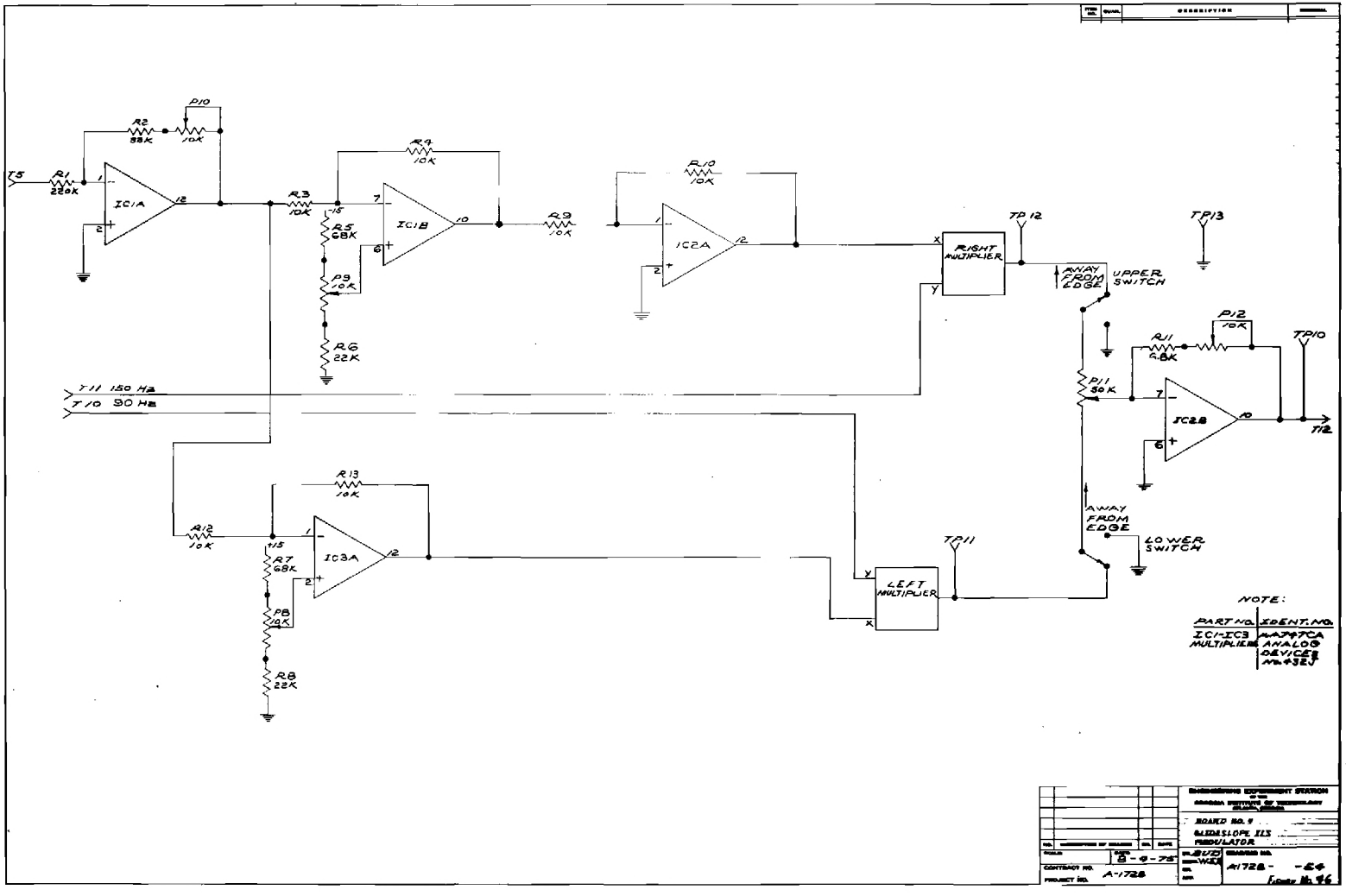


Figure 46. Schematic Diagram of Board No. 4.

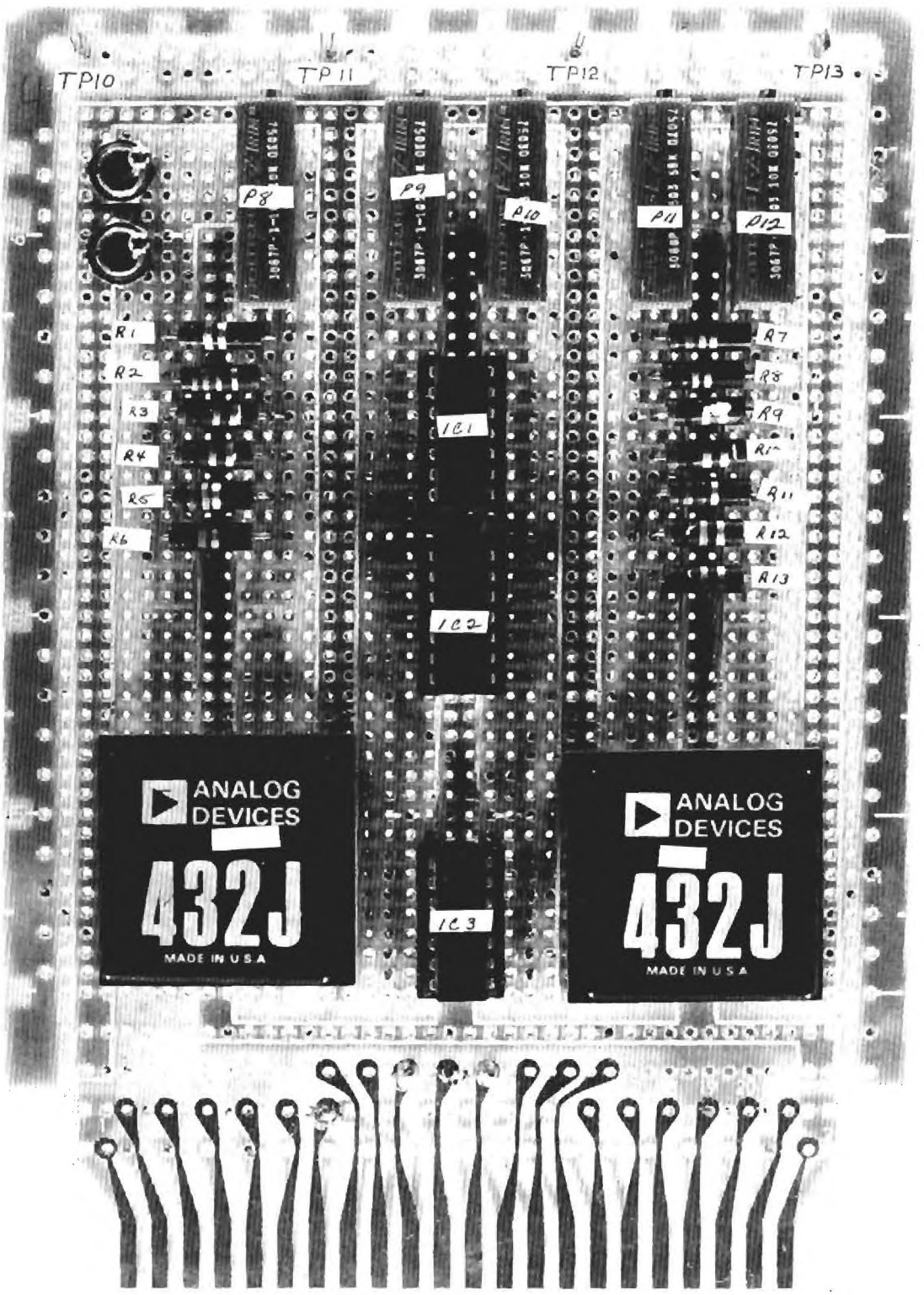


Figure 47. Component Identification Photograph of Board No. 4.

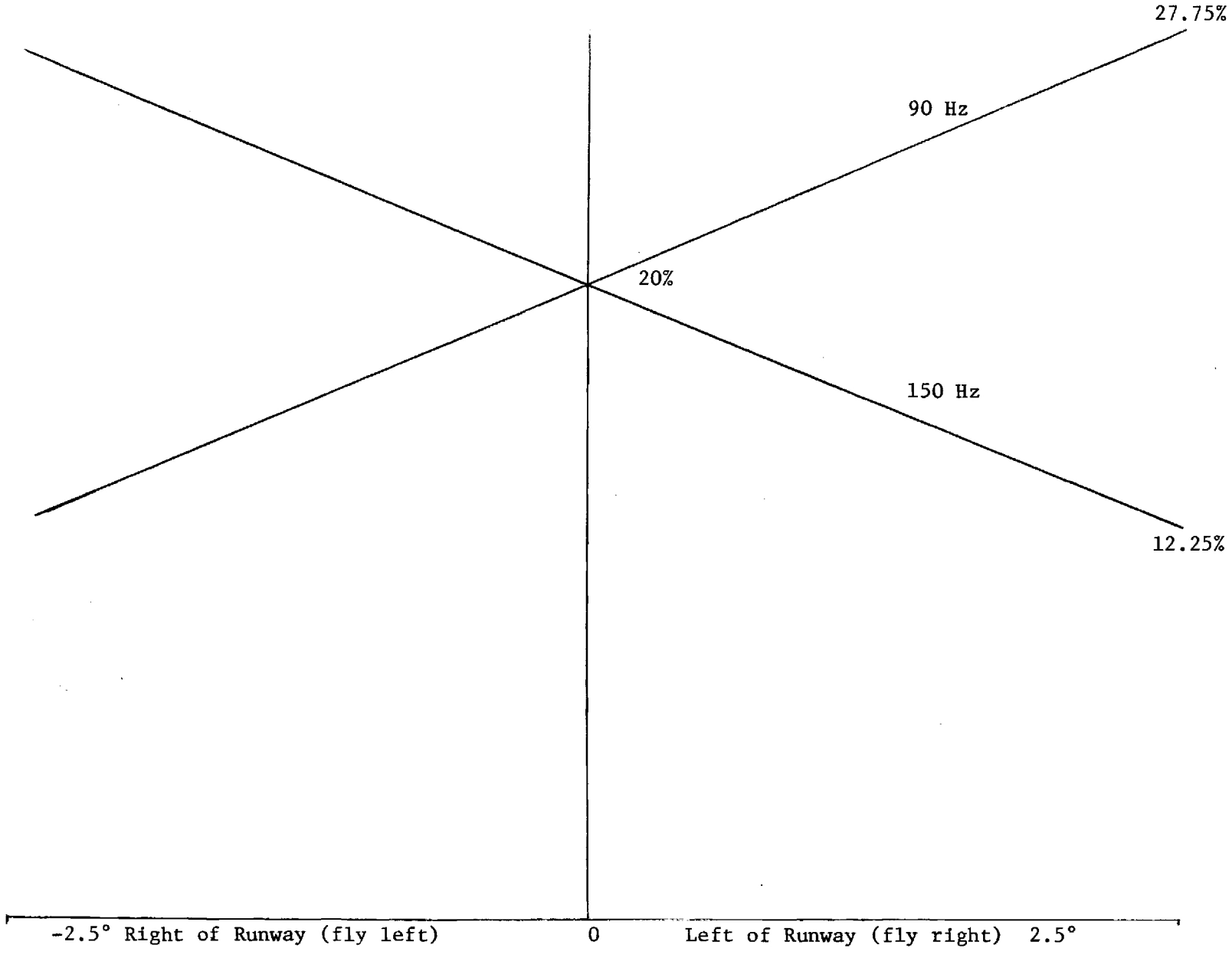


Figure 48. Courseline Transmitter Modulation vs. Aircraft Position

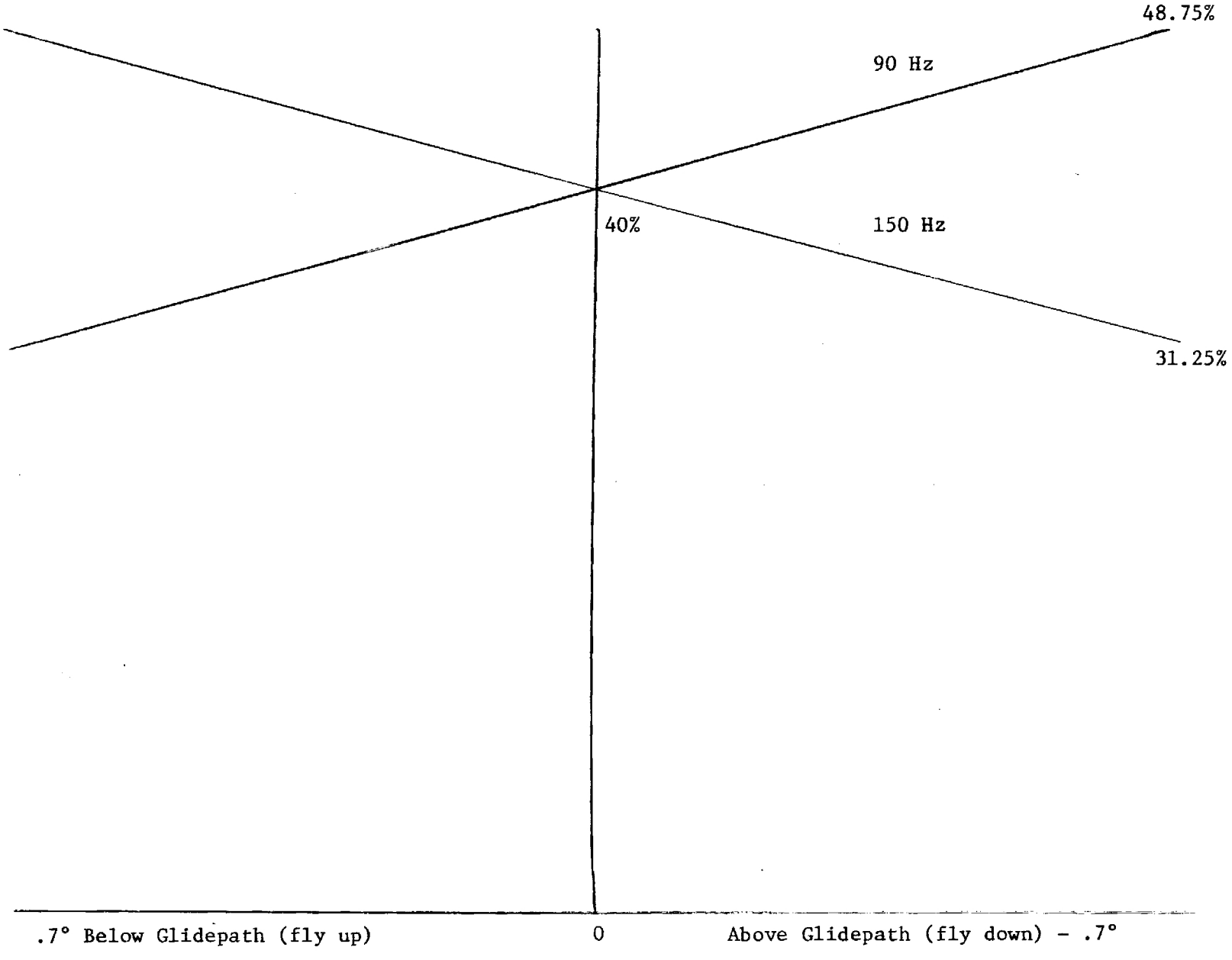


Figure 49. Glideslope Transmitter Modulation vs. Aircraft Position

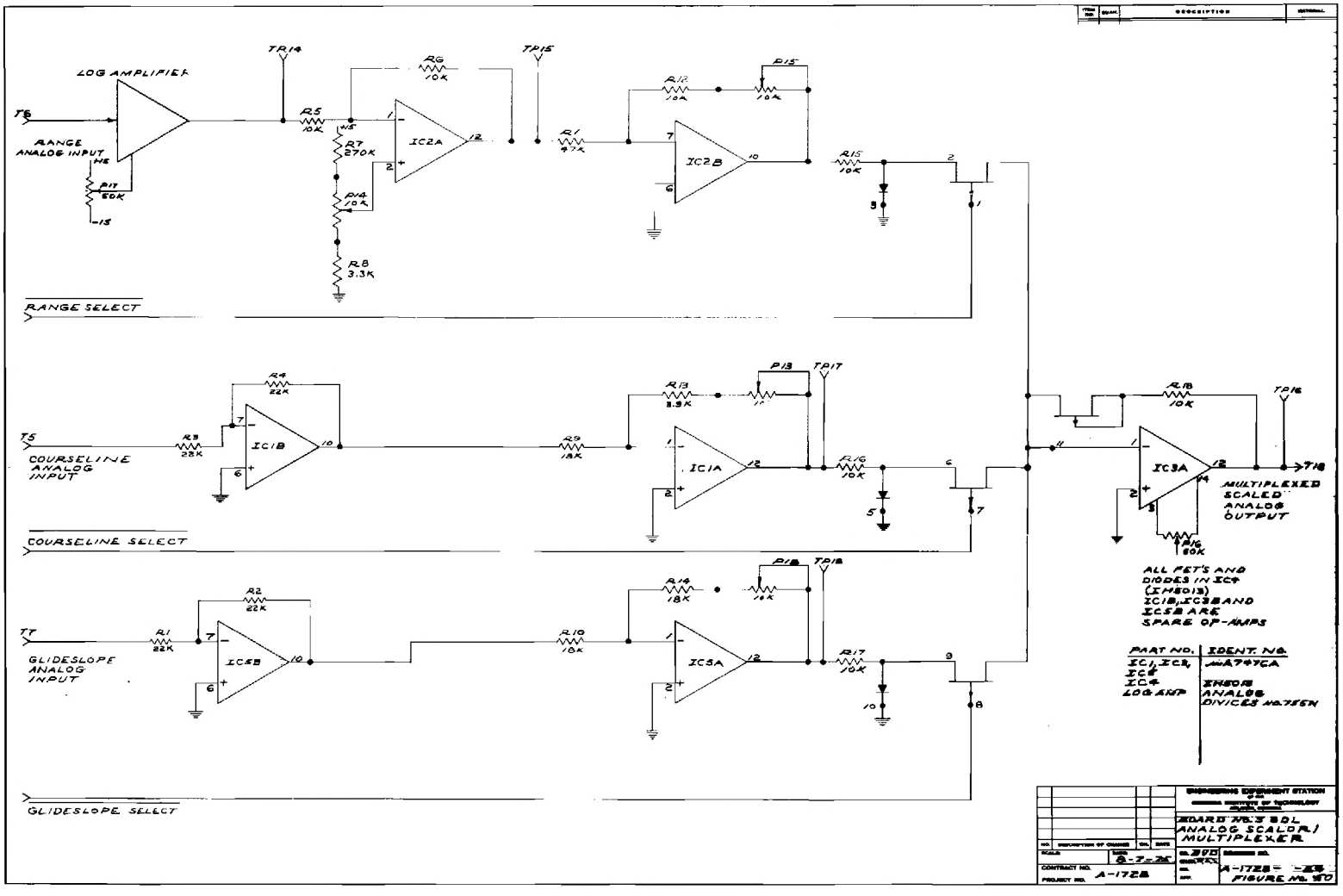


Figure 50. Schematic Diagram of Board No. 5.

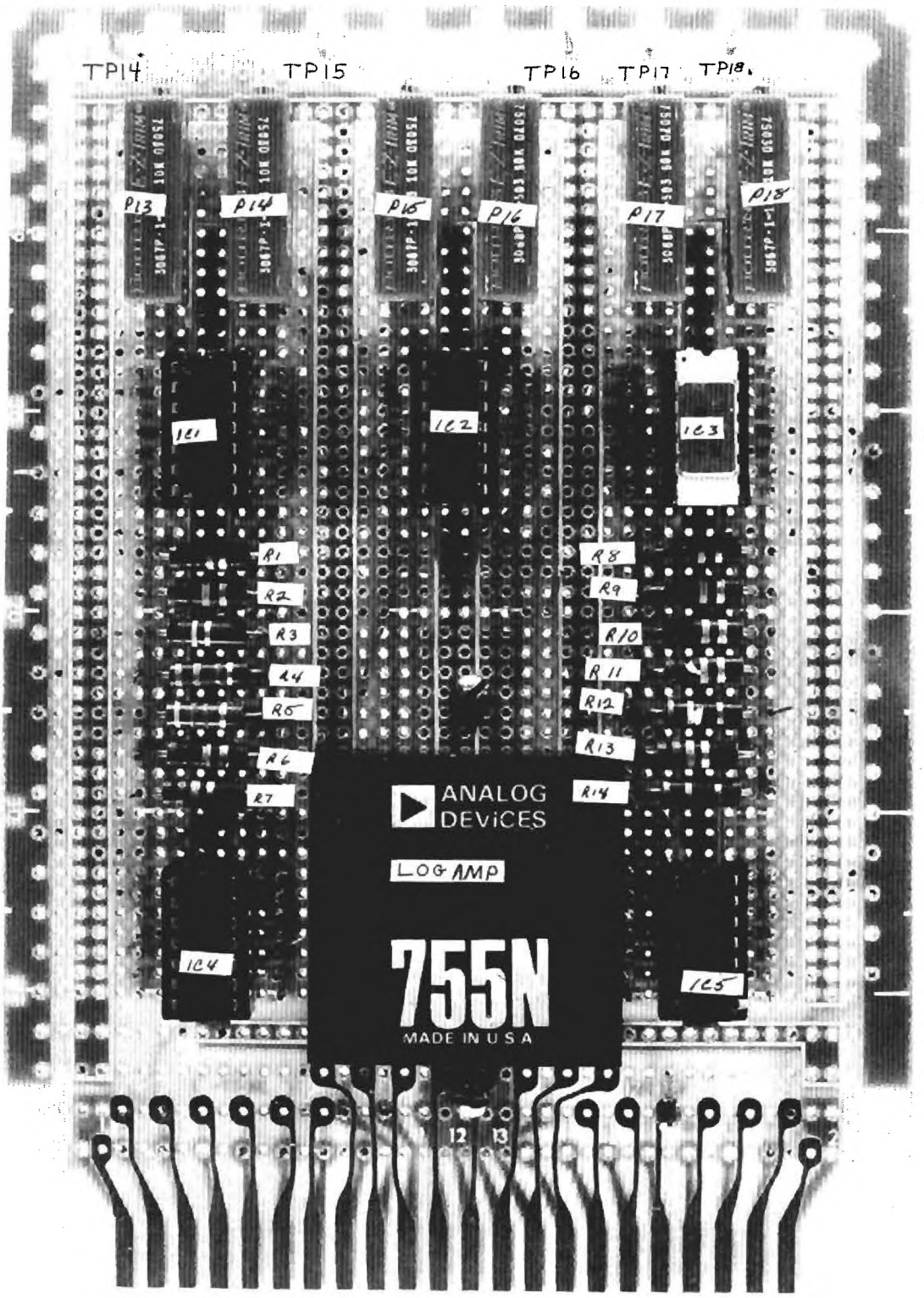


Figure 51. Component Identification Photograph of Board No. 5.

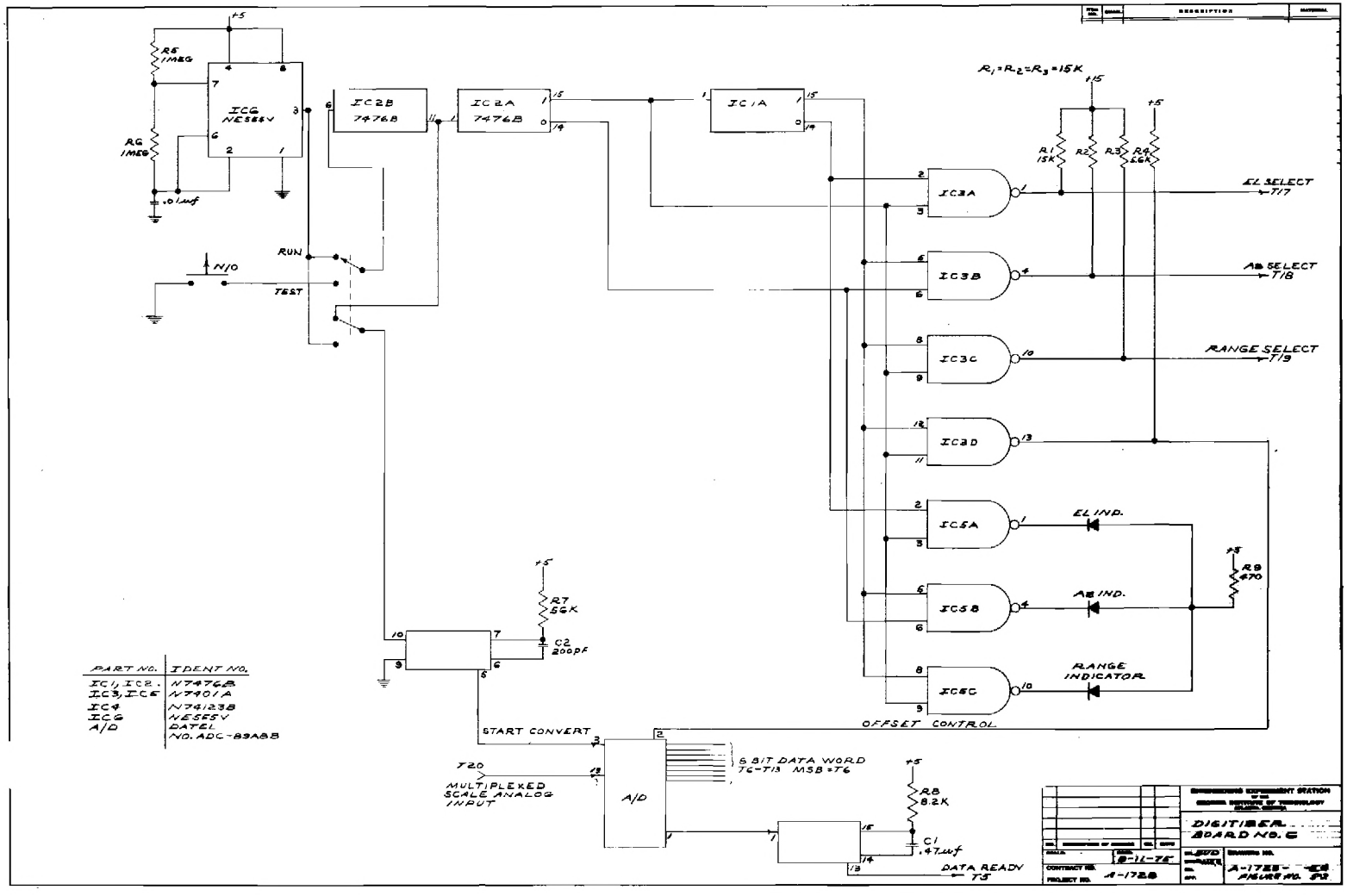
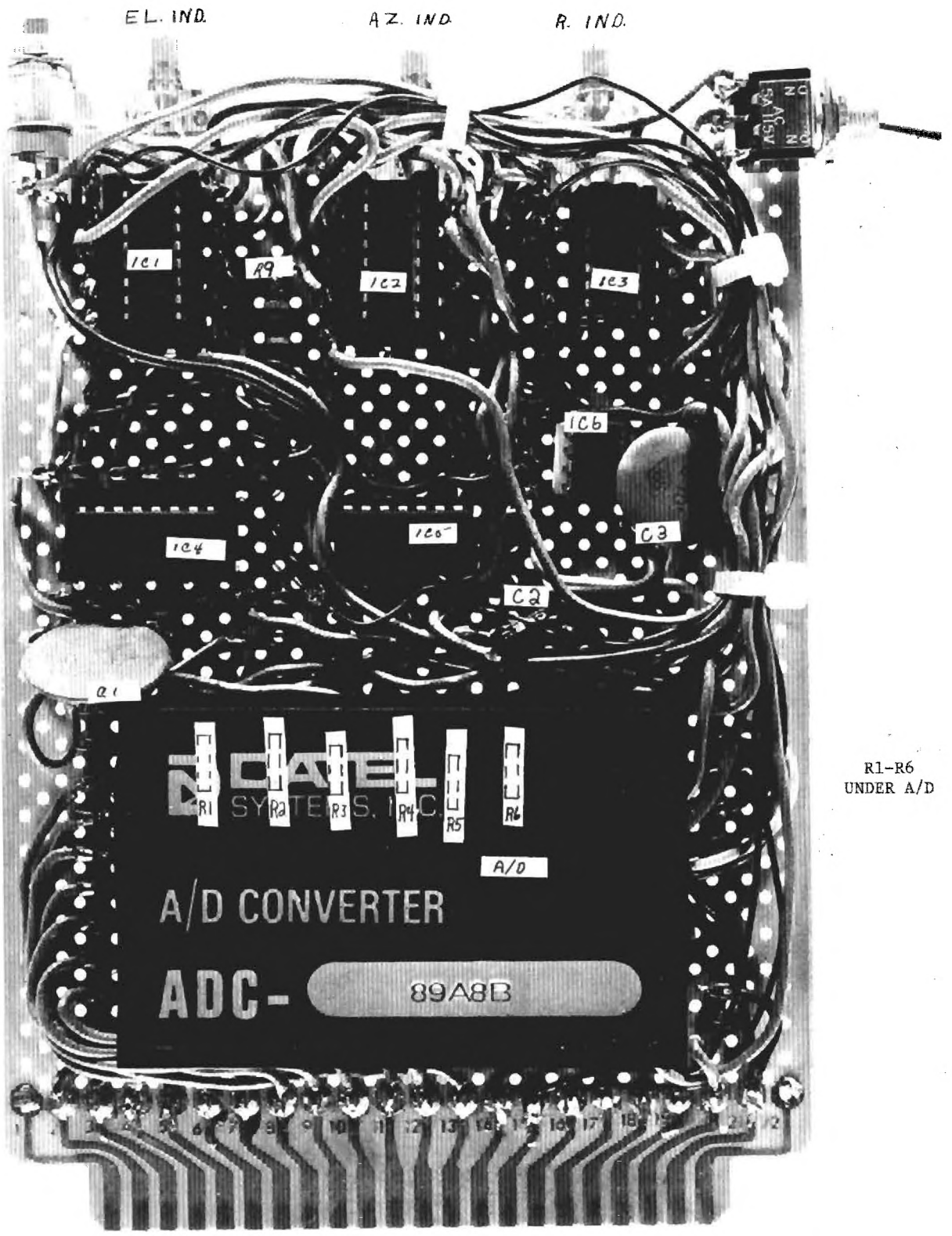


Figure 52. Schematic Diagram of Board No. 6.



R1-R6
UNDER A/D

Figure 53. Component Identification Photograph of Board No. 6.

The data selector generates the channel identification code (01 for elevation, 10 for azimuth, and 11 for range) with a two-bit binary counter clocked at sixteen Hertz. The outputs of the counter are decoded using NAND circuits to provide gating signals to the analog switches. Indicators on Board No. 6 reflect the state of the gating signals. The selected analog signal is applied to the A/D converter, and the 8 bit binary number is produced. At the end of conversion, the A/D converter generates an end-of-convert signal, which is converted to a pulse lasting for 13 ms. This pulse indicates to the Special Data Link that valid information is on the data lines. When the 16 Hz clock changes state, a new function code is generated and the cycle repeats. The binary number, the data ready pulse, the function code, and a fixed track code are isolated using opto-couplers as shown in Figures 5- and 7. The LED's on Board No. 7 display the binary number for calibration purposes.

5.3 Detailed Circuit Descriptions for Interface Units

5.3.1 Conventions and Common Features

5.3.1.1 Input/Output

Input and output signal flow is schematically shown with arrow tails and heads, respectively, with terminal numbers labeled with a "T". Brief word descriptions of the signals are given when necessary.

5.3.1.2 Component Symbols

Standard symbols are used for resistors, capacitors, diodes, transistors, relays, and simple analog integrated circuits such as amplifiers and comparators and digital integrated circuits such as NAND and NOR gates. Pin numbers are shown with the symbol. A very few special integrated circuits are used for simplicity. These are analog switches. Their individual components are shown as discretes; the group is then enclosed with a dashed line and appropriate notation given.

5.3.1.3 Component Identification

5.3.1.3.1 Junctions

Junctions between two components are clearly labeled with large darkened circles.

5.3.1.4 Waveforms

Liberal use of waveform sketches is made where it was felt they improved clarity. Polarity of DC voltages is given.

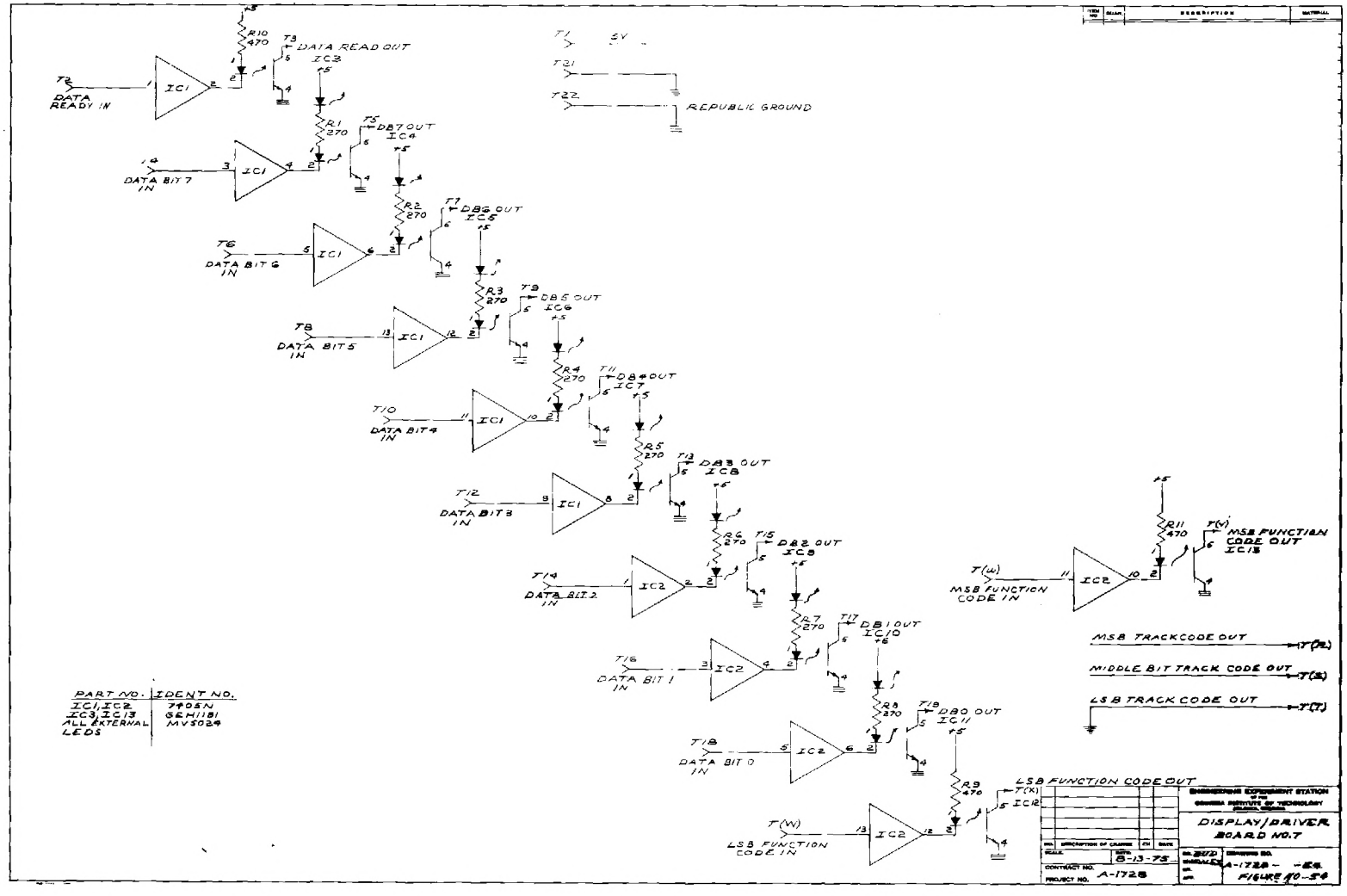


Figure 54. Schematic Diagram of Board No. 7.

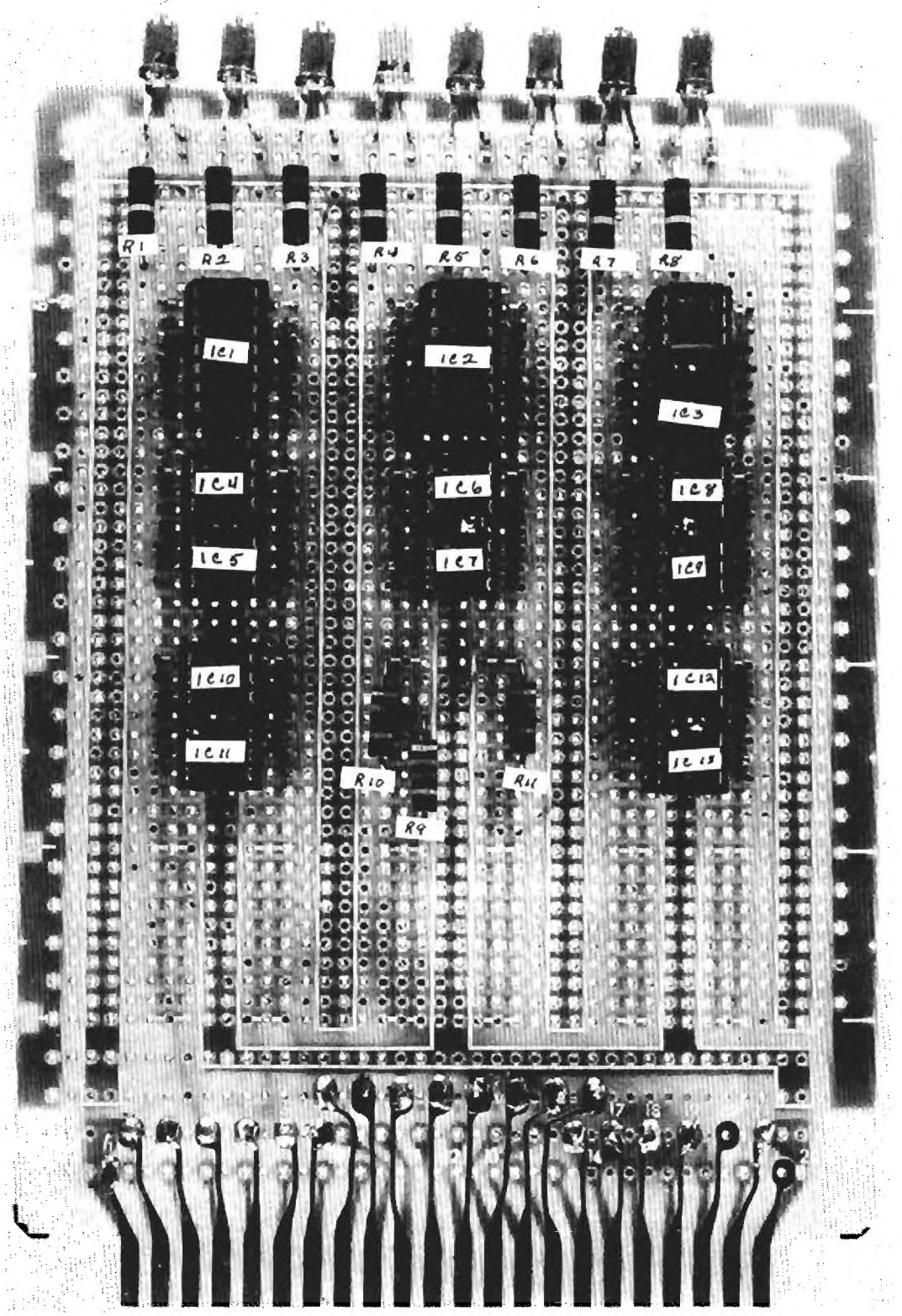


Figure 55. Component Identification Photograph of Board No. 7.

5.3.1.5 Component Identification

Resistors and capacitors in the signal flow path are labeled in close proximity to their symbol with an appropriate prefix and number, as well as their value. Diodes, transistors, and integrated circuits are labeled only with appropriate prefix (D, Q, and IC, respectively) and number, with their normal identification given in one or more notes on the drawing.

5.3.1.6 Power Supply Bus

Five voltage levels, including grounds, are required. Their respective terminals are common for each board except for the last two. The terminal-voltage correspondence is as follows:

T2	+15 volts
T3	-15 volts
T4	+5
T21	Interface ground
T22	SDL ground Board No. 7 and No. 8

These connections are not shown on the individual diagram.

5.3.2 Circuit Boards

The circuit boards upon which specific functions are implemented are identified in the lower left corner of each functional block in Figure 38.

Figures 50, 52, and 54 are schematic diagrams of the SDL section. The ILS section schematic is presented in four sections, with Figure 40 representing circuit Board No. 1, Figure 42 representing Board no. 2, and Figures 44 and 46 representing Boards Nos. 3 and 4. These schematics, together with the block diagram, are used to find the section (ILS or SDL), the board, the part number for a particular component. With this information, attention is directed to a schematic diagram and wiring harness diagram (Figure 56). Board I/O lists are given in Tables II-VII. Example: trace the 90 Hz square wave from the dividers through the filters, to amplification. Figure 38 shows that the dividers are on Board No. 1 and in the ILS section. Turning to Figure 40, note that the 90 Hz square wave leaves Board No. 1 via T6. The I/O list for Board No. 1 verifies this. Locate T6, Board No. 1 on Figure 40 and observe that it connects to T5 on Board No. 2. Figure 42 shows that T5 on Board No. 2 is the input to the 90 Hz filter. The signal emerges from the filter

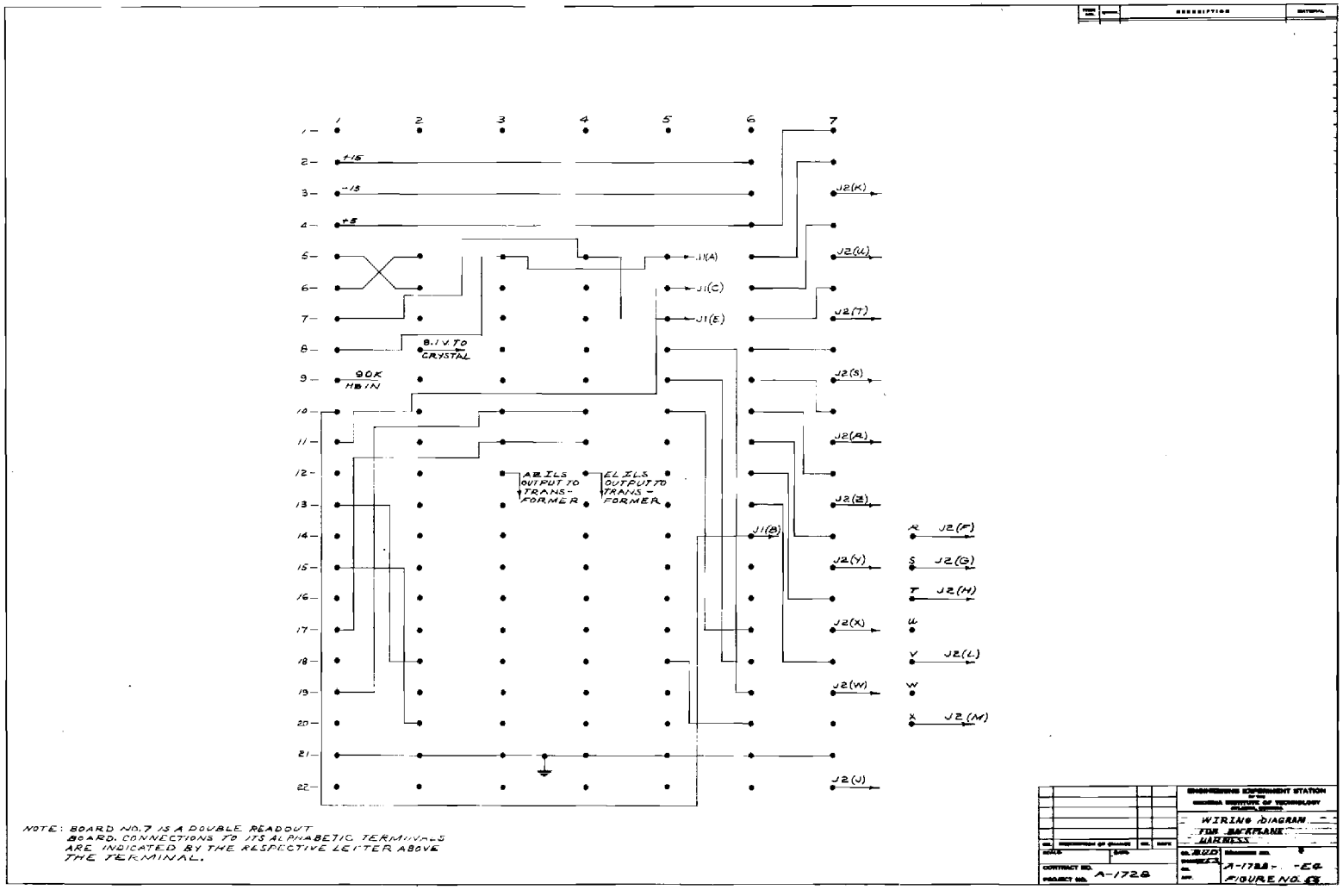


Figure 56. Wiring Diagram for Backplane Harness.

TABLE II

I/O LIST FOR BOARD NO. 1

1.
2. +15
3. -15
4. +5
5. 150 Hz Square wave output
6. 90 Hz Square wave output
7. EL Test Input
8. AZ Test Input
9. 90 kHz (from crystal oscillator) input
10. INTERFACE ENABLE (High on affirmative lock)
11. Range Test Input
12.
13. 150 Hz sine wave input (from filter, before amplification)
14.
15. 90 Hz sine wave input (from filter, before amplification)
16.
17. Amplified 150 Hz sine wave output
18.
19. Amplified 90 Hz sine wave output
20.
21. GND
22.

TABLE III

I/O LIST FOR BOARD NO. 2

1.	
2.	+15V
3.	-15V
4.	+5V
5.	90 Hz square wave input
6.	150 Hz square wave input
7.	
8.	+9.1V output for crystal ocillator
9.	
10.	
11.	
12.	
13.	
14.	
15.	
16.	
17.	
18.	150 Hz sine wave output (unbuffered)
19.	
20.	90 Hz sine wave output (unbuffered)
21.	GND
22.	

TABLE IV

I/O LIST FOR BOARD NO. 3

1.	
2.	+15V
3.	-15V
4.	+5V
5.	Az deviation input
6.	
7.	
8.	
9.	
10.	90 Hz sine wave input (10V p-p)
11.	150 Hz sine wave input 10V p-p)
12.	ILS - AZ - output
13.	
14.	
15.	
16.	
17.	
18.	
19.	
20.	
21.	GND

TABLE V

I/O LIST FOR BOARD NO. 4

1.	
2.	+15V
3.	-15V
4.	+5V
5.	EL deviation input
6.	
7.	
8.	
9.	
10.	90 Hz sine wave input (10V p-p)
11.	150 Hz sine wave input (10V p-p)
12.	ILS - EL - output
13.	
14.	
15.	
16.	
17.	
18.	
19.	
20.	
21.	GND
22.	

TABLE VI

I/O LIST FOR BOARD NO. 5

1.	
2.	+15V
3.	-15V
4.	+5V
5.	Az error input
6.	Range error input
7.	El error input
8.	$\overline{\text{RANGE SELECT}}$
9.	$\overline{\text{COURSELINE SELECT}}$
10.	$\overline{\text{GLIDESLOPE SELECT}}$
11.	
12.	
13.	
14.	
15.	
16.	
17.	
18.	Multiplexed Analog Output
19.	
20.	
21.	GND
22.	

TABLE VII

I/O LIST FOR BOARD NO. 6

1.
2. +15V
3. -15V
4. +5V
5. Data ready (from 1 shot) (Bit 8)
6. MSB data (Bit 7)
7. Bit 6
8. Bit 5
9. Bit 4
10. Bit 3
11. Bit 2
12. Bit 1
13. Bit 0
14. INTERFACE ENABLE
15. LSB function code (Bit 9)
16. MSB function code (Bit 10)
17. Analog Gate (EL) (outputs)
18. Analog Gate (Az)
19. Analog Gate (Range)
20. Multiplexed analog input
21. GND
22.

TABLE VIII

I/O LIST FOR BOARD NO. 7

1.	+5V	A	
2.	DATA READY IN	B	
3.	DATA READY OUT	C	
4.	DATA BIT (DB) 7 in	D	
5.	DB 7 OUT	E	
6.	DB 6 IN	F	
7.	DB 6 OUT	H	
8.	DB 5 IN	J	
9.	DB 5 OUT	K	
10.	DB 4 IN	L	
11.	DB 4 OUT	M	
12.	DB 3 IN	N	
13.	DB 3 OUT	P	
14.	DB 2 IN	R	MSB Track Code Out
15.	DB 2 OUT	S	Middle bit track code out
16.	DB 1 IN	T	LSB track code out
17.	DB 1 OUT	u	MSB function code in
18.	DB 0 IN	V	MSB function code out
19.	DB 0 OUT	W	LSB function code in
20.		X	LSB function code out
21.	Ground	Y	
22.	Republic Ground	z	

and leaves the board via T20. Returning to Figure 42, T20 on Board No. 2 connects to T15 on Board No. 1, which is the input to the 90 Hz amplifier as shown on Figure 40.

5.3.3 ILS Section Circuitry

The circuits of the tone generator, signal scalers, and the modulators and mixers used in the ILS section are described in the following.

5.3.3.1 Tone Generator (Figures 39 through 43)

The 90 KHz crystal oscillator is powered by a 9 volt regulator consisting of R9 and D1 on Board No. 2, and is located just in front of the power supply. The oscillator output is buffered by transistor Q1 and is applied to a two-input NAND gate. The Interface-Enable signal from the tracker is the other input to the gate. When Interface-Enable is high, 90 kHz is applied to the two divider chains. Integrated circuits IC1, IC2, IC3 and half of IC5 form a divide-by-1000 chain to yield a 900 Hz square wave. Integrated circuit 4 is decoded by 1/4 of IC6 (a NOR gate) to form a divide-by-3 counter which, together with IC5 forms a divide-by-6 counter. This divides the 900 Hz output of IC2 to produce a 150 Hz square wave.

These square waves are conducted to the low pass filters on Board No. 2. The 150 Hz filter has its corner frequency at about 160 Hz. Since the next harmonic present in the square wave is at 450 Hz (only odd harmonics are present) and therefore well into the stop band, essentially only the fundamental frequency of the square wave energes from the filter. The 90 Hz filter has a cutoff frequency of 100 Hz. The resultant sinusoidal voltages are conducted back to Board No. 1 where they are amplified by IC8, a dual operational amplifier. Gain adjustments for the 90 Hz and 150 Hz sinusoids are P1 and P2 respectively, on Board No. 1. The purity of the 90 and 150 Hz tones, and the relative phase between them are maintained to standards as dictated by the International Civil Aviation Organization, in the International Conference on Aeronautical Telecommunications, Annex 10.

5.3.3.2 ILS Scalers

The courseline scalers are composed of integrated circuits IC1, IC2, and IC3 on Board No. 3. These are μA747 dual operational amplifiers,

and the A or B suffix in Figure 44 indicates which half is being used. IC1A is connected as an inverting amplifier, with gain dependent upon the resistance of P4. This amplifier changes the magnitude of the slope of the input signal, and is directly coupled to IC2A. IC1A and IC3A are connected as unity gain amplifiers and do not modify the slope of the input signal (except to invert it), but simply add a constant voltage level to it. The 150 Hz component of the ILS signal requires a negative slope (as the deviation tends positive, the amplitude of the 150 Hz modulation decreases), and IC2A is connected to invert the output of IC1B, negating the inverting action of IC2A to form the inverting scaler channel. Integrated circuit IC3A behaves exactly as IC1B but its output is not inverted. This forms a noninverting stage, which is required to modulate the 90 Hz tone.

5.3.3.3 ILS Modulators and Mixers

The output of the inverting scaler modulates the 150 Hz tone and the noninverting scaler output modulates the 90 Hz tone, in two Analog Devices #432J multipliers. The modulated 90 Hz and 150 Hz tones are mixed together in IC2B, to form the composite courseline ILS signal, which is applied to a 600 ohm 1:1 transformer. The transformer is used to provide a balanced output.

The glideslope ILS channel operates exactly as the courseline channel, but slope and constant settings are different.

5.3.4 SDL Section Circuitry

The circuits for the SDL section range and angle scaler amplifiers and the data selector/binary counter are described in the following.

5.3.4.1 Range Scaler

The range voltage entering T6 of Board No. 5 is applied directly to the log amplifier input, since they are already compatible. Operational amplifier IC2A and IC2B form a post scaler to adapt the log amplifier output to the A/D converter input. As seen from Figure 57, the log amplifier output is related to its input by $V_o = -1 - \log_{10} (V_{in})$ for K = 1. Operational amplifier IC2A inverts the output of the log amplifier and adds 1 volt. The relationship between the log amplifier input and IC2A's output becomes $V_{out} = 2 + \log_{10} (V_{in})$. Typical input-output pairs are:

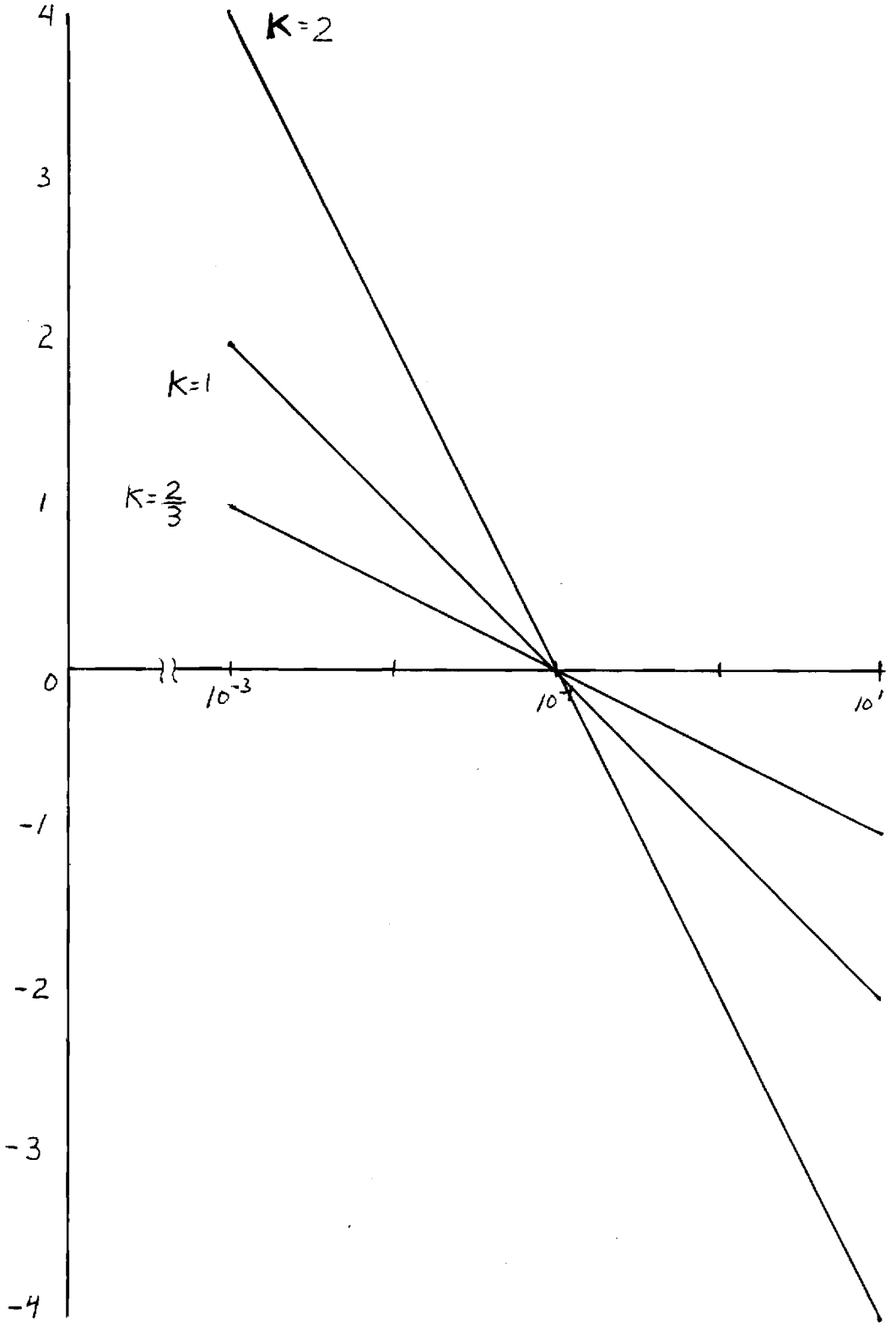


Figure 57. Log Amplifier Transfer Function

Input (V)	Output (V)
10^{-2}	0
10^{-1}	1
10^{0}	2
10^{1}	3

These are scaled in IC2B such that when a voltage corresponding to 10 nmi is applied to the chain, all bits of the A/D go to the one state.

5.3.4.2 Courseline and Glideslope Scalers

The courseline and glideslope scalers are used to attenuate the range of analog voltage from the tracker to -5 to +5 volts for presentation to the A/D. The scalers are in an inverting configuration to negate the effect of the analog switch buffer. Calibration of these scalers is such that $+2.5^{o}$ courseline deviations or $+.7^{o}$ glideslope deviation turns all data bits on. Positive courseline deviation is defined as a fly right indication (aircraft to left of center). Positive glideslope deviation is defined as fly up (aircraft below glide path).

5.3.4.3 Data Selector/Binary Counter

In the normal mode, the two bit binary counter (IC2A and IC1A, Board No. 6) is clocked at a 16 Hz rate by the 32 Hz free-running multivibrator IC6, on Board No. 6 which is divided in half by flipflop IC2A on Board No. 6. At this clock frequency, the aircraft will receive full update (range, azimuth, and elevation) four times per second; this is within the Special Data Link capacity requirement of two to six times per second. The "1" outputs of the counter form the function code bits for the special data link.

The data selector is made up of four NAND (IC3, A6) which decode the outputs of the two-bit counter. The outputs of the gates are normally high, but when the proper function code occurs, the gate corresponding to the function code will drop to approximately zero volts. When the gate is low the corresponding analog switch is turned on, and the analog voltage is delivered to the A/D converter. The inputs of IC5 are in parallel with those of IC3 so that IC5 decodes the same states as IC3. The outputs of IC5 drive three indicators to display the state of the data selector.

One of the four NAND gates is connected to place a logic "1" on pin 2 of the A/D when the function code for range occurs. This allows the A/D to operate in straight binary mode during the range interrogation cycle, and offset binary during courseline and glideslope interrogation cycles. Four microseconds after

one of the analog switches is energized, a start-convert pulse is delivered to the A/D converter by the one-shot, IC4A. This delay allows time for the analog switches to settle before the A/D begins to convert. When the A/D has completed its conversion, the end-of-convert output goes low. Integrated circuit one-shot IC4B responds to this transition and produces a pulse approximately 13 ms long which is the data-ready pulse for the Special Data Link. If the interface-enable signal is low, the process above is inhibited. No data ready pulse is produced, and the function code sets to 00.

In the test mode, the output of the 32 Hz clock is taken from the divide-by-two flipflop and placed onto the input of IC4, a one shot with the "1" output connected to the start convert input of the A/D converter. The signal that normally triggers this one shot is disconnected. This delivers start-convert pulses to the A/D at a 32 Hz rate, which causes the A/D to convert at 32 Hz. A normally open SPST pushbutton switch is connected between the divide by two flipflop input, and ground. Floating the input of this flipflop has the effect of applying a logic "1" to it. The flipflop responds to trailing edges, so when the pushbutton is depressed, the flipflop changes state. In this way the data selector may be manually clocked, to connect any scaler output with the A/D converter at will. The digital output of the selected analog input is displayed on the Light Emitting Diodes (LEDs) on Board No. 7.

TABLE IX

PIN CONNECTIONS FOR THE SDL OUTPUT CONNECTOR (J2)
AND THE DATA INPUT CONNECTOR (J1)

J2		J1	
A	Spare	A	Courseline Input
B	Spare	B	Interface Enable
F	Channel Code MSB	C	Range Input
g	Channel Code Middle Bit	E	Glideslope Input
H	Channel Code LSB	F	Ground
J	Return		
K	Data Ready		
L	Function Code MSB		
M	Function Code LSB		
P	Return		
Q	Return		
R	Data Bit (DB) 4		
S	DB5		
U	DB7		
V	Return		
W	DB Ø		
X	DB 1		
Y	DB 2		
Z	DB 3		

SECTION VI

INTERFACE UNIT ALIGNMENT PROCEDURE

6.1 Alignment and Calibration for the ILS Section

6.1.1 Tone Amplitude Adjustments

Disconnect the input connector (J1) from the interface and turn the power switch "on." Adjust P1 and P2 on board No. 1 for 10 volts (peak-to-peak) on test points TP4 and TP5.

6.1.2 Courseline Channel Scale Settings

Set P6 to midrange and be sure that both toggle switches are pointing away from the board edge. Ground TP2 and adjust P3 and P4 for 7.21 volts (peak-to-peak) on TP7 and TP8, respectively. Apply +10 V to TP2 and adjust P5 for 10 volts (peak-to-peak) on TP7. Ground TP2 and connect the courseline ILS output to its respective ILS transmitter input. Energize the courseline transmitter and adjust P7 until the transmitter is modulated approximately 30 percent. Using the toggle switches to apply 90 to 150 Hz separately to the transmitter (the upper switch corresponds to 150 Hz), adjust P6 such that equal modulation results from the two tones. The actual modulation level is not important; (except that it should not exceed 100 percent) the purpose of this step is to achieve a balance of equal RF modulation for zero input to the board. After balance is obtained, adjust P7 so that the modulation level is exactly 20 percent. The courseline channel is now calibrated.

6.1.3 Glideslope Channel Scale Settings

Set P11 to midrange and be sure that both toggle switches point away from the board edge. Ground TP1 and adjust P8 and P9 for 8.21 volts (peak-to-peak) on TP11 and TP12, respectively. Apply +10 volts to TP1 and adjust P10 for 10 volts (peak-to-peak) on TP11. Ground TP1 and connect the glideslope output to its respective ILS transmitter input. Energize the glideslope transmitter and adjust P12 until the transmitter is modulated approximately 30 percent. Using the toggle switches to apply 90 to 150 Hz separately to the transmitter (the upper switch controls 150 Hz), adjust P11 such that equal modulation results from both tones (balancing step). After balance is achieve, adjust P12 so that the transmitter is modulated exactly 40 percent. The glideslope channel is now calibrated.

6.2 Alignment and Calibration for the SDL Section

6.2.1 Range Channel

Apply 10 volts to TP3 and adjust P17 for exactly -2 volts on TP14. Position the test switch lever down and press the pushbuttom as many times as necessary until the LED closest to the rear of the cabinet turns on. Adjust P14 until +3 volts are read on TP15. Adjust P15 until all LED's on Board No. 7 are on. The range channel is now calibrated.

6.2.2 Courseline Channel

Apply 10 volts to TP2 and with the test switch lever in the downward position, press the pushbutton as many times as necessary until the middle LED is on. Adjust P13 until all LED's on Board No. 7 are on. The courseline channel is now calibrated.

6.2.3 Glideslope Channel

Apply 10 volts to TP1 and with the test switch lever in the downward position, press the pushbutton as many times as necessary until the LED closest to the front of the board turns on. Adjust P18 until all LED's on Board No. 7 are on. The glideslope channel is now calibrated.

6.3 ILS Modulation vs. Aircraft Position

The relationships between the ILS 90 Hz and 150 Hz modulation levels and angular deviation from the ideal approach path are derived as follows. It is known [1] that (1) the modulation level of both the 90 Hz and the 150 Hz signals is 20% on the ideal approach path; (2) the Difference in Depth of Modulation (DDM) at full scale ILS deviation is 15.5%; (3) the 150 Hz modulation predominates the right of the runway (pilot's view), and the 90 Hz dominates to the left.

Along a vertical plane located 2.5 degrees left of the runway, the 90 Hz modulation is greater than the 150 Hz by 15.5%. Assuming ideal (linear) change in each modulation level with courseline deviation, the 90 Hz modulation index is

$$M90 = 20 + (3.1)\ X\ [\text{percent}],$$

where X is the aircraft deviation (degrees to the left of the runway. The equation describing the 150 Hz modulation index is

$$M150 - 20 - (3.1)\ X\ [\text{percent}].$$

A similar pair of results holds for the glideslope channel modulations:

$$M90 = 40 + (17.5/1.4)\ Z\ [\text{percent}],$$

$$M150 = 40 + (17.5/1.4)\ Z\ [\text{percent}],$$

where Z is the aircraft elevation deviation in degrees. Figures 11 and 12 portray graphically the courseline and glideslope modulation indices as functions of aircraft angular deviation.

SECTION VII
FLIGHT TEST RESULTS

7.1 Introduction

The Tracking Unit and Interface Unit were flight tested during the period 19-22 August 1975 at the Naval Electronic Systems Test and Evaluation Detachment (NESTED). Analysis of the data recorded during these tests indicate that the Tracking Unit and Interface Unit, when interfaced with the AN/TPN-8 and the Republic Electronics UHF Data Link, can provide guidance information to an aircraft that is adequate for Mode II landings provided that the aircraft is on a clutter free approach path in clear weather.

7.2 Test Set-Up

The pertinent radar, tracker, aircraft and environmental parameters are listed in Tables X, XI, XII, and XIII, respectively.

7.3 Qualitative Flight Test Results

The results of the passes are summarized below by category.

7.3.1 Target Acquisition

No difficulty was encountered in this area provided that the target was not in heavy ground clutter at the acquisition point.

7.3.2 Target Tracking

No problems in this area except for regions of intense ground clutter. In these regions, the azimuth and elevation IF gains required adjustment to avoid clutter lock-ons. This is an area which needs to be addressed in any future work.

7.3.3 Azimuth Data

The data was generally smooth, and the pilot had no difficulty in following the azimuth needle. A few isolated cases of "needle chasing" were reportedby the pilot at ranges of 2.0 nautical miles or less. These instances correlate generally with the few cases of azimuth gate pull-off due to ground clutter.

TABLE X

RADAR PARAMETERS

Pulsewidth	800 nonoseconds*
Power Setting	1/2 Power
Video Level	4.0 volts average
If Noise Level	1.0 volts average
Elevation If Gain	Variable
Azimuth IF Gain	Variable
STC	On
FTC	On

Offsets From Nominal Touchdown	
x	5000 feet (down range)
y	180 feet (offset)
z	Nominal Antenna Height

TABLE XI

TRACKER PARAMETERS

Video Threshold	2.3 volts
Acquisition Gate Widths	
Range	2.0 microseconds
Azimuth	12.0 degrees
Elevation	4.4 degrees
Tracking Gate Widths	
Range	0.5 microseconds
Azimuth	1.5 degrees
Elevation	1.5 degrees
Tracking Loop Gains	
Range	Not Recorded
Azimuth	Not Recorded
Elevation	Not Recorded
Number of Hits to Acquire (threshold setting)	Not Recorded
Track Drop Delay	Not Recorded
Data Rate	1 Hz

TABLE XII

AIRCRAFT PARAMETERS

Cessna 402 Twin Engine		
	Airspeed	120 Knots (Average)
	Video Return	Comparable In Magnitude to F-4 and A-7 returns

TABLE XIII

ENVIRONMENTAL CONDITIONS

Clear	
Minimum visibility to 3.0 nautical miles in haze at times	
Winds	Negligible

7.3.4 Elevation Data

Due to higher indicator angular sensitivity and approximately the same rms error, the data appeared somewhat noisier than in the azimuth channel. Several successful needle approaches were accomplished (without clutter lock-on) by careful manual adjustment of the elevation IF gain control.

7.3.5 Range Data

The recorded data was very smooth and accuracy was verified by voice checks with aircraft to compare ground indicator readings with airborne indicator.

7.4 Quantitative Flight Test Results

A total of 10.2 flight hours were flown on 55 passes of which 30 were for purposes of orientation. Of the 25 passes in which an attempt was made to transmit guidance signals, 10 were accomplished with azimuth needle only and 15 were made with full azimuth, elevation, and range information.

7.4.1 Absolute Accuracy

No independent monitor was available to employ as a reference for absolute accuracy determination. However, ground observations of the aircraft breaking out over runway threshold and pilot observations during the approach indicated no serious system misalignments or bias errors in the tracking system.

7.4.2 Relative Accuracy

Table XIV reflects the indicated azimuth errors in degrees from a predetermined courseline as derived from strip chart recordings of the error taken at the radar site for five different approaches at one nautical mile intervals from 6 nautical miles down to 1 nautical mile. Table XV gives the same data in terms of distance (feet) from the desired courseline. Tables XVI and XVII reflect similar information for the elevation data.

TABLE XIV

AZIMUTH ERROR (DEGREES)

RANGE (N. MILES)	FLIGHT NUMBER 1	2	3	4	5
6	.375	1.875	2.375	1.125	.25
5	.125	0	.625	2.0	.875
4	.4	1.0	.625	1.0	.25
3	.25	.5	.5	.44	.375
2	0	.125	.375	.125	.125
1	.25	.25	1.50	.25	.25

TABLE XV

AZIMUTH ERROR (FEET)

RANGE (N. MILES)	FLIGHT NUMBER 1	2	3	4	5
6	196	1181	1535	669	157
5	65	0	328	1050	459
4	183	420	288	420	105
3	78	157	157	118	137
2	0	26	78	26	26
1	26	26	164	26	26

TABLE XVI

ELEVATION ERROR (DEGREES)

RANGE (N. MILES)	FLIGHT NUMBER 1	2	3	4	5
6	.385	.525	.315	.42	.315
5	.14	.14	.045	.105	.07
4	.035	.14	.105	0	.175
3	.07	.035	.045	.07	.045
2	.105	.035	.07	.14	.035
1	.07	.14	.087	.14	.14

TABLE XVII

ELEVATION ERROR (FEET)

RANGE (N. MILES)	FLIGHT NUMBER 1	2	3	4	5
6	242	330	187	275	198
5	82	64	27	55	45
4	22	58	36	0	73
3	27	11	16	16	16
2	22	11	18	29	7
1	7.3	16	9	14	14

SECTION VIII

CONCLUSIONS AND RECOMMENDATIONS

The investigations reported herein have demonstrated that successful Mode II approaches can be made when using the Georgia Tech Tracker/Interface in conjunction with an AN/TPN-8 radar system and the Republic Industries UHF Data Link. Additional flight testing, however, and further research is indicated to address the following areas:

1. Optimum Acquisition Gate Widths,
2. Optimum Tracking Gate Widths,
3. Optimum (Adaptive) Loop Gains,
4. Optimum AN/TPN-8 Radar Video Processor Settings for Clutter Suppression,
5. Absolute Accuracy Checks,
6. Pseudo ILS Flight Tests, and
7. Foul Weather Tracking.

REFERENCES

1. "Technical Manual for Digital Data Link," Research Communications Industries, Burlington, Massachusetts, 26 January 1973.

SECTION VIII
CONCLUSIONS AND RECOMMENDATIONS

The investigations reported herein have demonstrated that successful Mode II approaches can be made when using the Georgia Tech Tracker/Interface in conjunction with an AN/TPN-8 radar system and the Republic Industries UHF Data Link. Additional flight testing, however, and further research is indicated to address the following areas:

1. Optimum Acquisition Gate Widths,
2. Optimum Tracking Gate Widths,
3. Optimum (Adaptive) Loop Gains,
4. Optimum AN/TPN-8 Radar Video Processor Settings for Clutter Suppression,
5. Absolute Accuracy Checks,
6. Pseudo ILS Flight Tests, and
7. Foul Weather Tracking.

REFERENCES

1. "Technical Manual for Digital Data Link," Research Communications Industries, Burlington, Massachusetts, 26 January 1973.

DISTRIBUTION LIST

Office of Naval Research 800 N. Quincy Street Arlington, VA 22217 Code 211 (CDR R. P. Hite)	3
Office of Naval Research Branch Office 536 South Clark Street Chicago, IL 60605	1
Office of Naval Research Resident Representative Georgia Institute of Technology Hinman Building Atlanta, GA 30332	1
U. S. Naval Research Laboratory Washington, DC 30275 Code 2627 Code 2629	 6 6
Defense Documentation Center Bldg. 5 Cameron Station Alexandria, VA 22314	12
U. S. Naval Electronic Systems Command Washington, DC 20361 Code 5403 (Mr. R. Wilz) Code 520A (Mr. E. Nordenburg)	 5 2
U. S. Naval Electronics System Test and Evaluation Detachment Naval Air Station Patuxent River, MD 20670 Code 022 (Mr. P. Hopkins)	2
U. S. Marine Corps Headquarters Washington, D. C. 20380 Code AAM (Mr. A. Warnack)	2
Naval Systems Engineering Center Vallejo, CA 94562 Code W041 (Mr. F. Stokhan)	2
Marine Corps Development Center Air Branch Fire Power Division Quantico, VA 22134 Code D091 (Mr. E. Thomas)	2
Republic Electronics Industry Corp. 575 Broadhollow Road Melville, NY 11746 Attn: W. C. Oehrle	1